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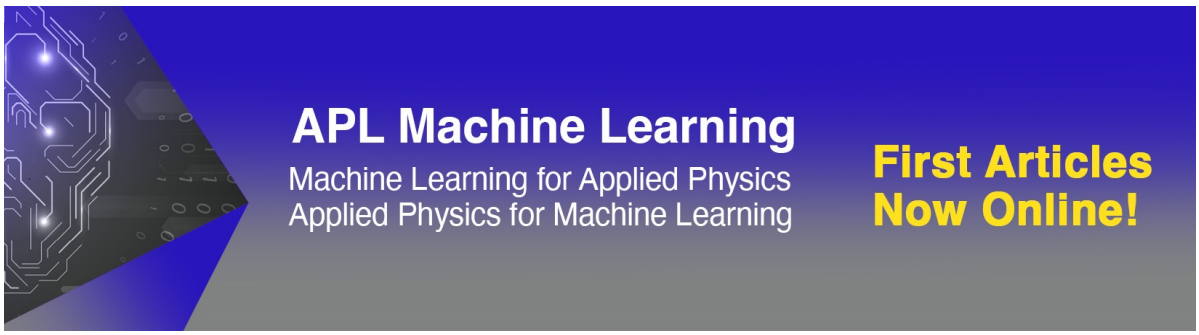
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ABSTRACT

Quantum key distribution (QKD) has rapidly developed recently. The repetition frequency of the QKD system increases from tens or hundreds of MHz to GHz. A laser diode (LD) operating in gain-switched mode is widely used as a weak coherent light source in a QKD system. We present an LD driver circuit fabricated in 0.18 μm SiGe heterojunction bipolar transistor bipolar complementary metal oxide semiconductor technology. The circuit can operate at frequencies up to 2.5 GHz, satisfying the requirements of high-speed laser drives in practical QKD systems. The output current of the driver circuit can reach 100 mA when driving an LD whose input equivalent resistance is ~21 Ω. The extinction ratio of the 1550-nm distributed feedback LD light source driven by our driver circuit reaches 23 dB at the operating frequency of 2.5 GHz, meeting the requirements of QKD systems. This circuit will be used in miniaturized QKD systems.

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I. INTRODUCTION

Quantum key distribution (QKD) provides secure communication based on quantum physics, and it has rapidly developed recently. Bennett and Brassard proposed the first QKD protocol named the BB84 protocol in 1984.[1] The first QKD demonstration experiment, published in 1991,[2] operated at a communication distance of 32 cm. More recently, a space-to-ground QKD experiment relying on the Micius satellite has been realized.[3] A space-to-ground integrated quantum communication network has already been established, and the communication distance can go up to thousands of kilometers.[4] Meanwhile, to ensure the security of QKD using realistic devices, different protocols[5–7] have been proposed and some methods[8,9] have been investigated to solve the deviation of realistic devices from the idealized model. QKD emanated from the laboratory and has moved to large-scale practical applications. The code rate of QKD systems is important in practical applications, so the repetition frequency of QKD systems in practical applications gradually increases from tens or hundreds of MHz to GHz.

The QKD systems are mainly composed of discrete optical and electronic devices.[10,11] As QKD moves toward practicality, to apply it in more scenarios, miniaturization of the system is becoming important. We intend to miniaturize the entire sender of the QKD system. Co-packaging of integrated photonics and electronics is a solution

for miniaturization of the QKD system. Our work has been carried out for integrated photonics and integrated electronics, and some results have been achieved at the frequency of 312.5 MHz.[12] This paper focuses on the LD driver for high speed application, and it is a step in integrating the entire sender electronics into one chip.

The application of our driver circuit is based on the scheme of the decoy-state BB84 protocol that is widely used in QKD systems.[13] In the sender part of the scheme of the decoy-state BB84 protocol, a weak coherent light source needs to emit periodic optical pulse signals, which are modulated to three different intensity states and then modulated to four polarization states through the modulator. The modulated optical signal needs to be attenuated to single photon level by an attenuator and then sent to the receiver via an optical fiber or free-space channel. A 1550-nm distributed feedback (DFB) LD is usually used as a weak coherent light source in QKD systems[12,13] due to its low costs and low attenuation in both optical fiber and free space media.[14,15] Our driver circuit is designed for the 1550-nm DFB LD for which the equivalent resistance when operating at GHz is ~21 Ω (including series protection resistors in the LD package). Optical amplification techniques cannot be used for transmission in the quantum channel. The extinction ratio of the laser output optical signal in the QKD system should be higher than 20 dB, which is much higher than that in traditional optical communication. A high extinction ratio means that the average photon number of the vacuum state in the intensity modulation of the optical pulse is closer to zero, and the risk of vacuum state information leakage is reduced. Additionally, a high extinction ratio also results in a low system bit error ratio. We designed the LD driver using a 130 nm complementary metal-oxide semiconductor (CMOS) process with an operating frequency of 625 MHz.[16,17] There are no internal matching resistors at the output of the driver circuit to keep the output voltage swing in line with the process requirements. While for operating frequency of GHz and driving current in excess of 100 mA, the parasitic effects of the transistors have a significant impact on the output signal,[18] and the reflection of the signal due to the absence of matching resistors cannot be ignored. CMOS process does not meet our needs. Electrical driver, for output voltage over 3 V, has been primarily done in compound semiconductors.[18] This is mainly due to breakdown limitations of silicon transistors and large required voltage swing.[19] However, silicon has advantages in heat dissipation, cost, and compatibility with CMOS processes.[20] The control and reference modules operating at low speeds can still be designed with MOS transistors in bipolar complementary metal oxide semiconductor (BiCMOS) technology. This paper introduces a cascode topology with two kinds of npn heterojunction bipolar transistor (HBT) that overcomes the breakdown limitations of the transistors by design and enables high-speed broadband drivers with a large voltage swing in silicon. In this paper, we present a silicon germanium (SiGe) BiCMOS circuit for driving laser sources to emit optical pulses that can meet the requirements of QKD systems with 2.5 GHz repeating frequency.

II. CIRCUIT DESIGN

Differential mode has a significant advantage in suppressing noise and electromagnetic interference compared with single-ended mode, and the output current can be more stable. Although the LD operates in single-ended drive mode, we used a differential circuit structure in the design of the entire driver chip, and the other terminal of the differential output is connected to a dummy resistance. The overall structure of the laser driver chip designed in this paper is presented in Fig. 1. The current mode logic (CML) module receives the logic control system's trigger signal, and the signal's pulse-width can be adjusted through the pulse-width control (PWC) module. Then, the driving capability of the signal is provided by the pre-amplify module, and finally, the output stage is capable of outputting the current pulse signal.

A. Characteristics of laser

To obtain the required optical signal from an LD, the simulation of LD rate equations[21] that model the electrical and optical performance of an LD was studied. The parameters in the LD rate equations are from a typical LD. From the simulation results, it can be found that a narrow current pulse signal is needed to drive LD to operate in gain-switched mode so as to obtain a narrow optical pulse signal. As shown in Fig. 2(a), when the pulse-width of the driving current is fixed, if the amplitude of the driving current is too small, the luminous intensity of the LD is relatively weak. By increasing the current amplitude, a narrow and intense optical pulse signal is generated; however, as the drive current amplitude is further increased,

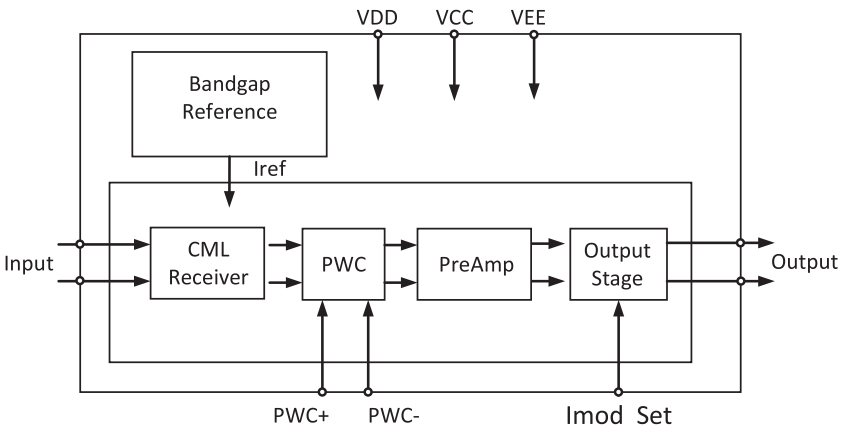


FIG. 1. Structure of laser driver.

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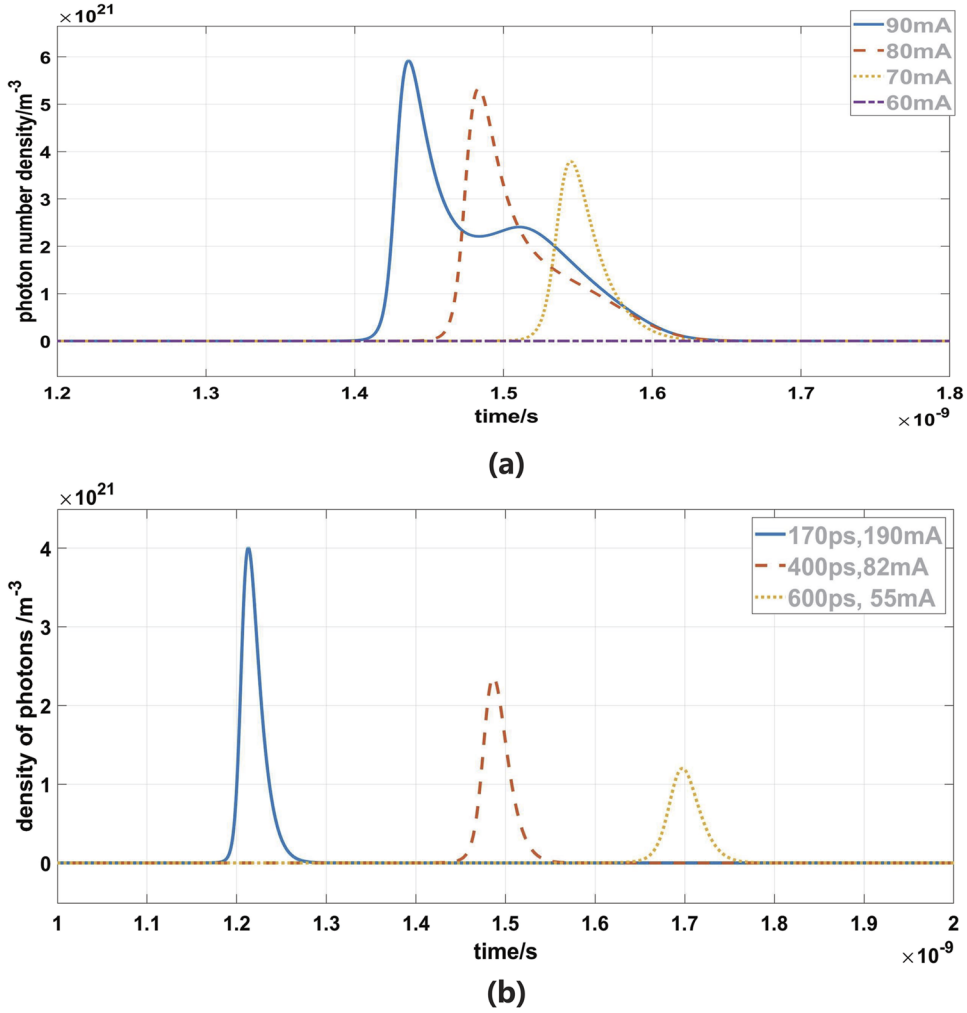


FIG. 2. (a) Optical signal vs different current amplitudes at a given pulse-width. (b) Optical signal vs different pulse-widths with corresponding current amplitude.

the optical pulse becomes wider. The simulation results of the narrow optical pulse signal obtained using different pulse-widths of the drive current are shown in Fig. 2(b). It can be found that a narrower current pulse-width corresponds to a larger current amplitude, and simultaneously, narrower optical pulse-width and higher intensity are obtained. Therefore, the current amplitude of the driver's output should be adjusted precisely, and the driver must be able to output current pulse signals with high bandwidth and large current amplitude. According to the test condition of the adopted DFB LD, the maximum driving current amplitude is set to 100 mA in our design.

Unlike the requirements of conventional optical communication drivers, the LD biased near the threshold current will emit weak fluorescence, resulting in phase correlation of the output optical signal, leading to safety problems in the QKD systems.[22] Therefore, the laser driver does not have a module that provides a DC bias current. The driver should be completely shut down as soon as the output corresponds to a zero optical signal.[23]

B. Input and pulse-width control module

The chip's input interface circuit receives the digital signal from the prior stage, which then sends it to the PWC module in the following stage. At an operating frequency of up to 2.5 GHz, a minimum output electrical pulse-width of 200 ps is required. In the above simulation, it can be found that different optical pulse-widths and intensities correspond to different electrical pulse-widths and intensities. In practical applications, we need to generate current pulses of different pulse-widths. Since the data rate of the CML receiver module is enough to receive a 200 ps pulse-width signal, the laser driver does not need an additional narrow pulse generation module presented in article.[16] The pulse-width of the output signal is mainly determined by that of the chip's input signal's pulse-width controlled by the prior stage. The pulse-width only needs to be adjusted slightly on chip.

The diagram of the PWC module is shown in Fig. 3. The design principle is to introduce an externally controlled offset voltage at the input of the second-stage differential pair, causing the difference in

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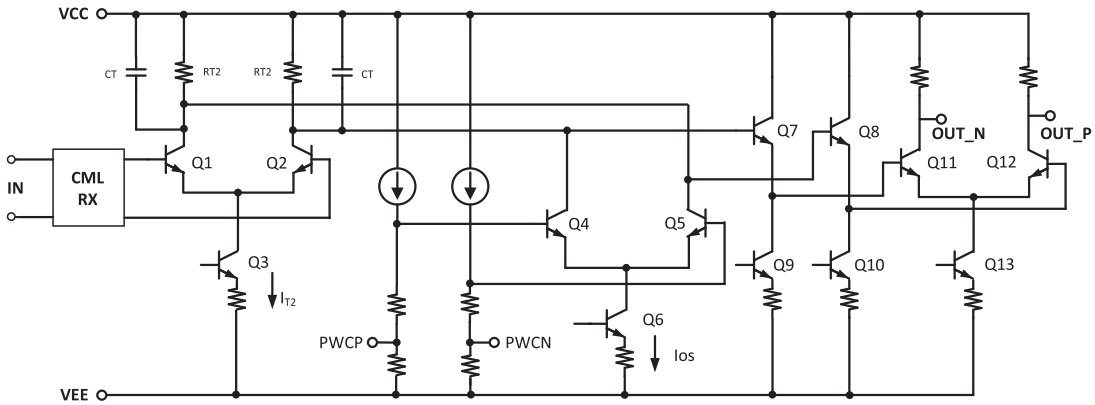


FIG. 3. Schematics of the input and PWC module.

the common-mode levels of the two output signals of the previous-stage differential pair. The larger the value, the larger the duty cycle deviation of the output signal of the second stage. In this design, a capacitor is selected in parallel at the load end to slow down the slope of the signal. By controlling the voltages of the pulse width control-positive (PWCP) and pulse width control-negative (PWCN) ports in Fig. 3, the adjustment range of the pulse-width can reach ~33 ps. Continuous adjustment can be realized by means of an external sliding resistor connected between PWCP port and PWCN port.

C. Preamplification

To drive a large modulation current (up to 140 mA), the size of the switching npn HBTs of the output stage is so large, thus introducing a large capacitance. Therefore, the output resistance of the pre-amplify stage for which driving the output stage's switching transistors must be minimal to reduce the time constant of pre-amplify stage's output node. Additionally, when the switching transistor of the output stage is switched, there is a spike switching current, and according to the simulation results, the peak of this current is approximately between 1/3 and 1/4 of the internal modulation current of the output stage. The pre-amplify stage needs to provide the instantaneous switching current to make the output stage's switching transistors switch quickly. Therefore, a multistage emitter–follower cascade structure is usually adopted to reduce the output resistance and provide the large instantaneous current required for the switching of the output stage's transistors, ~30–40 mA in this design.

The base voltage increases when the output stage's transistor switches are turned on, necessitating a current flow path. At this point, the emitter–follower transistors allow the current to pass from the power source to the base of the switching transistors. When the switching transistors are closed, the instantaneous current flows out of the base of the switching transistors through the bias current source of the emitter–followers. The DC bias current source of the emitter–follower provides the outflow path at the moment when the output switch is turned off. Such a large bias current of the emitter follower is wasted when the output switch is turned on, resulting in low utilization of the bias current. Considering the moment of switching the differential transistors, when one is on and the other is off. Then, a synchronous switch can be introduced to control the large bias current of the emitter–follower, allowing the bias current to be supplied mainly to the emitter–follower that is in the off state. Figure 4 depicts the circuit diagram of the pre-amplify stage using a dynamic bias structure, with npn in the form of a diode connection omitted.

Parasitic inductance brought on by the metal wiring of the circuit may have a considerable effect on the circuit performance, necessitating specific treatments.[24] Figure 5 depicts a diagram of the pre-amplify stage considering the influence of the parasitic inductance of the metal connection. Since the output of the emitter–follower transistors Q5 and Q6 are connected to the base of the output stage's switching transistors, which have a large parasitic capacitance. At the moment of switching, there is a large and fast instantaneous current pulse peak in the emitter–follower transistor Q5 and Q6's output terminal, and a rapid current pulse is formed in the collector of Q5 and Q6. Even if the parasitic inductance of the connection between the collector and the power source is small (tens of pH), a significant and quick voltage fluctuation will result from this. A feedback path is created by the parasitic capacitance of the collector junctions of Q3 and Q4 and the load resistance of the preceding stage. The fluctuation voltage is feed back to the output terminal of the common–emitter differential pair Q3 and Q4 of the preceding stage, that degrades the output signal's quality and, in extreme cases, results in oscillation.

Given that the switching states of Q5 and Q6 and the currents running through them at the time of switching are opposing, the differential structure can reduce the spike current to the power source from parasitic inductance L_V. By connecting their collectors, the currents can be complementary, so it is essential to reduce the parasitic inductance of the connection between Q3 and Q4. However, even if the inductance L_D is 0 nH, the switching effect cannot be completely eliminated due to the asymmetry of the transistor's on and off state. Therefore, it is also necessary to reduce the value of L_V. By introducing the parameters of these parasitic inductances in the presimulation, it can be discovered that the parasitic inductance L_R between the prior load resistances and emitter–follower transistor Q5 (and Q6) has more influence than the parasitic inductance (L_D) of the connection between the prior load resistances.[24] A negative real part of the transmitter–follower's input impedance is

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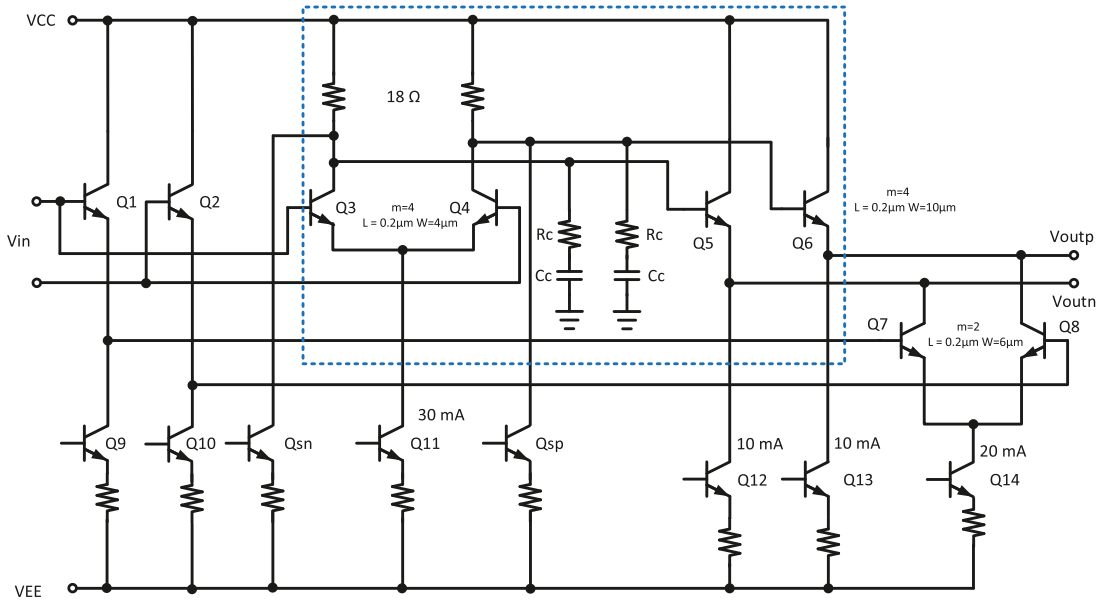


FIG. 4. Schematics of the pre-amplify stage.

easy to cause oscillation when the load capacitance is too large, and an RC compensation circuit is connected in parallel to the input of the emitter–follower.

Given these contributing considerations, the pre-amplify scheme uses the matching layout in Fig. 5 rather than the customary

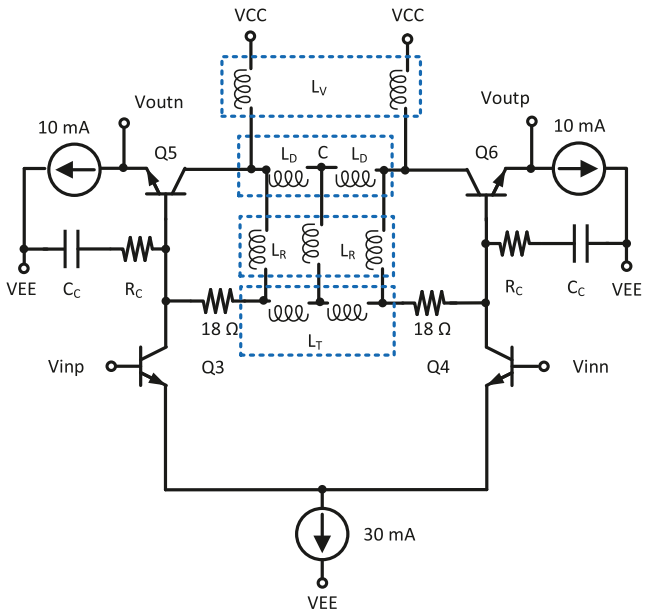


FIG. 5. Simplified circuit diagram of the driver with parasitic inductance of the local ground-supply metallization in the pre-amplify stage.

differential layout. The L_R and L_D values are considerably reduced by dividing the differential circuit into two symmetrical up and down sections and using a large metal plane as the power plane in the middle of the differential circuit. We introduce a big power metallization area surrounding the core driver circuit in the layout design, adding multiple power pads, and reducing the values of L_V. A significant number of coupling capacitors are added to the power plane during layout design to lessen the impact of the inductance L_V. The layout significantly lessens the impact of the power supply's parasitic inductance in applications requiring high currents compared to the conventional differential circuit layout.

D. Modulation current adjustable current driver

The circuit diagram of the output stage of the laser driver in this paper is shown in Fig. 6. The application requires a maximum internal modulation current of 140 mA, with a load resistance of 50 Ω and the 50 Ω characteristic impedance of the transmission line, and the maximum voltage swing is ~3.5 V. When the transistor works in high-speed mode, the HBT collector–emitter cross-voltage needs to exceed the cross-voltage of the linear resistance region of the transistor by a sufficient voltage margin. Based on the behavioral simulation of transistors of the process we used, a relatively large cross-voltage is needed for transistors operating in high speed mode. Additionally, the influence of the parasitic resistance on the output path, the voltage division of the bond wire inductance during the transient change of the current, the impact of overshoot, and the cross-voltage V_{ce} of the output stage's transistors need to be ~5 V to ensure a safe voltage margin.

In the process we used, there are two kinds of npn HBTs, and their breakdown voltages BV_{CEO} are, respectively, 1.6 and 3.2 V. When these two transistors were used in the driver circuit design,

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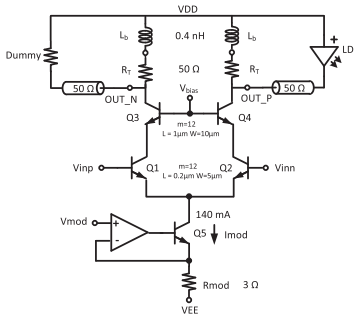


FIG. 6. Schematics of the output stage.

they were not used in the open base circuit structure. The parameter BV_{CER} of the HBT is the breakdown voltage when the base of the transistor is connected to resistor R. BV_{CER} is related to the breakdown voltage parameter BV_{CEO} provided by process documentation by the following equation:

$$BV_{CEO} = BV_{CER}(R = \infty) < BV_{CER} < BV_{CER}(R = 0). \quad (1)$$

Along with prior research on the breakdown voltage of the two HBTs used in this paper, which differ from the widely used cascode structure,[25] the transistors in the common–base stage use HBTs with slower speed and higher BV_{CEO}. This kind of HBT can withstand a large voltage swing across the output terminal over 5 V. Because of the lower across-voltage required, faster HBTs with a lower BV_{CEO} are used in the common–emitter switching stage. The cascode stage's output time constant is roughly provided by[26]

$$\tau_Q = [C_{\pi 1} + C_{\mu 1}(1 - A_{vQ1})](R_1 + r_{\pi 1}) + R_{eff}(C_{TQ3} + C_{ML} + C_{PAD} + C_{RT}). \quad (2)$$

Here, R_1 is the output resistance of pre-amplify stage. The input capacitance and resistance of Q1 are, respectively, $C_{\pi 1}$ and $r_{\pi 1}$. $C_{\mu 1}$ represents the base to collector capacitance of Q1. A_{vQ1} is Q1's base to collector amplification ratio. R_{eff} denotes the output stage's effective load resistance. C_{TQ3} is the whole collector capacitance of Q3. The capacitance of a PAD is C_{PAD}. C_{ML} denotes the capacitance of the internal metal. The internal termination resistor's capacitance, or C_{RT}, has a value of several hundred fF. The use of a cascode structure reduces A_{vQ1} from roughly seven to approximately one, and the transistor's capacitance $C_{\pi 1}$ brought on by the use of high-speed HBTs with high current density is also significantly reduced, which can greatly reduce the input capacitance when compared to the direct use of high-cross-voltage differential pair switching transistors.

Inductor introduces a zero to extend the bandwidth of output stage. Since the bond wire is inductive, we can use the bond wire as peaking inductance to steepen pulse edges.[27] The output eye diagram is degraded at peaking inductances that are too high,[26] the HBTs operate in large-signal mode, and a precise value of inductance is not required. Therefore, we make the two matching resistors connected separately to the external power supply through the bond wires. The drawback of this topology is that it increases the power supply noise due to the interference of inductance. However, the power supply noise can be isolated by insulating the output stage's power supply from the circuit's preceding stages. The output stage's power supply is simultaneously disconnected from the previous stages, and the power supply voltage of the output stage can be changed according to the magnitude of the modulation current. When the modulation current is small and the output swing is small, the power supply voltage of the output stage can be reduced from 5.5–6.5 to ~3–4 V, which significantly saves power consumption. Additionally, reducing the power supply voltage of the output stage when the modulation current is small can ensure safe operation of the transistor.

Because the optical power of the LD's output varies with temperature, the driver's output current needs to be controlled externally to compensate for this variation. It is necessary to control the bias voltage of the tail internal modulation current transistor to control the current output by the driver. Assuming that the bias voltage directly controls the base voltage of the tail current transistor, it is difficult to precisely control the current due to the nonlinear output curve of the transistor current. In this circumstance, a small change in the base voltage will result in a huge change in the modulation current (a change of 60 mV at room temperature will cause a tenfold change in the current).

The entire area of a single transistor in the HBT process is constrained due to the size of the output stage's transistors, and the larger the area of the HBT's emitter (with a given width), the more likely it is that the carrier injection effect brought on by avalanche breakdown will occur.[28] Therefore, each transistor in the common–emitter stage and the common–base stage is divided into 12 transistors to form four arrays, and the current tail transistor is divided into 24 transistors to form an array. We present two topologies to prevent the current disturbance of each transistor array, where most of the current is concentrated in the transistors in the middle of the transistor array.[29]

First, considering 1 mV in V_{be} for each transistor will cause a 2% difference in current. An uneven current distribution in the array will result from a tiny layout mismatch. However, the mismatch in V_{be} produced by the parasitic resistance of the wiring connecting the transistor array's emitters will have a greater effect, will have a negative impact on the case of excessive current, and may lead to a transistor burning out if the current exceeds the design tolerance. Therefore, in this design, an emitter degeneration resistor is introduced in each common source stage (CSS) array transistor as depicted in Fig. 7, and the resistor's negative feedback function reduces the mismatch of the transistor current in the CSS array caused by the mismatch of the wire's layout.[30] Simultaneously, substrate contacts are made around each transistor in the array to reduce the threshold mismatch caused by the substrate contact resistance.

The temperature of the inner transistors is higher than that of the outer ones when the circuit is functioning, which may cause most current to flow only via the center transistors. To get around this issue, we use the topology shown in Fig. 7. The collectors of each transistor in the common base stage (CBS) transistor array are connected together as the output port, their emitters are linked to each transistor collector in the CSS transistor array, and the emitters of the transistors in the CSS array are connected to each emitter-degradation resistance. They are then connected to separate tail

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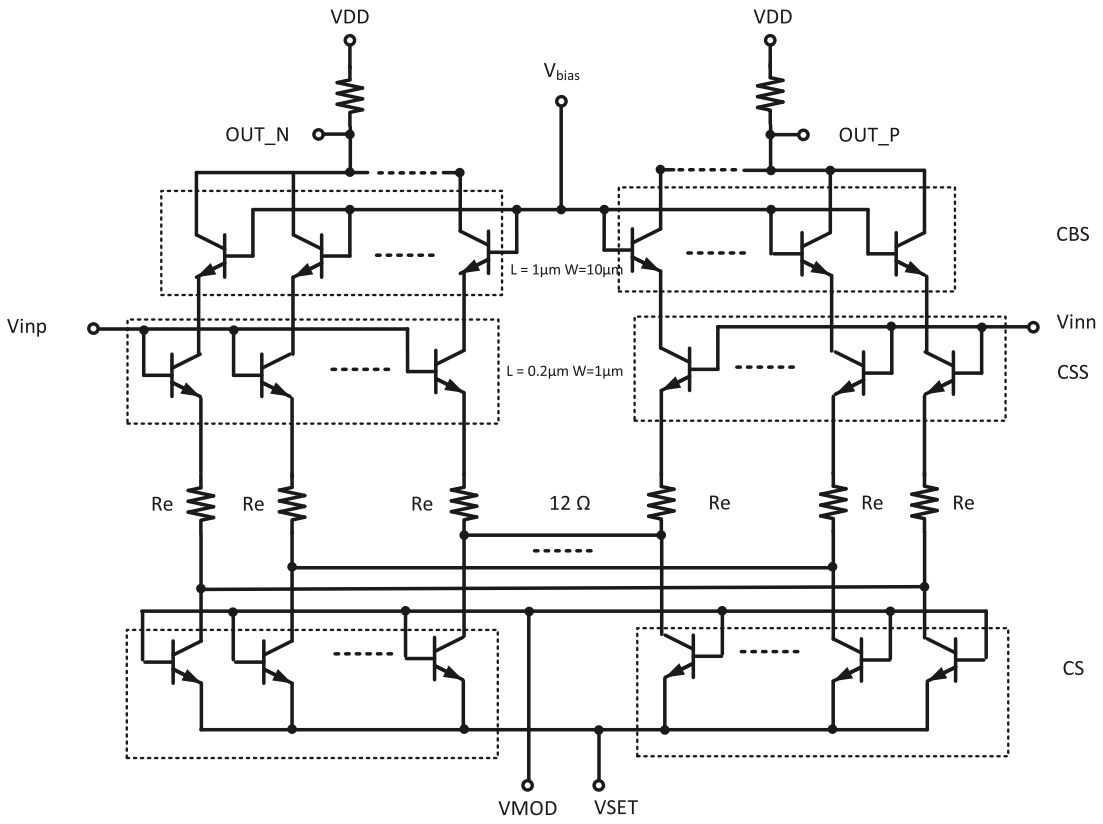


FIG. 7. Schematics of the output cascode stage designed with the consideration of the current hogging prevention concept.

current transistors in the current source (CS) transistor array. It prevents an average dispersed current from being concentrated in the inner transistors of each array by this topology.

III. CIRCUIT IMPLEMENTATION AND MEASUREMENT RESULTS

The circuit was fabricated using 0.18 μm SiGe BiCMOS technology. The chip size is 1330 × 1630 μm^2, and Fig. 8 depicts the chip micrograph. The 4 × 4 mm^2 square flat no-lead (QFN) package used by the packaged driver has an exposed pad that aids heat dissipation. The driver's current output port is on the right side of the package, and the input port is on the left. The chip is located on the right side of the package to reduce the length of the output bond wire to ~0.3 mm. Additionally, the output adopts a double bond wire to reduce the inductance value of the bond wire by ~35% compared to a single bond wire. The error in the length of the bond wire can be precisely controlled by the manufacturer within 20%, which meets our requirement. For testing, the chip is soldered on a multilayer printed circuit board (PCB), where it receives signals and produces driving current signals via an small A type (SMA) connector. A large number of ground bond wires and multiple vias in the PCB under the driver package help reduce the inductance of ground bond wires and improve heat dissipation of the chip. The output pins are connected to the signal layer of the PCB. In order to improve the matching performance, the lower layer of the signal layer is the voltage of device (VDD) layer, and the characteristic impedance of the signal transmission line is 50 **Ω**, which is equal to the on-chip resistance, to achieve impedance matching.

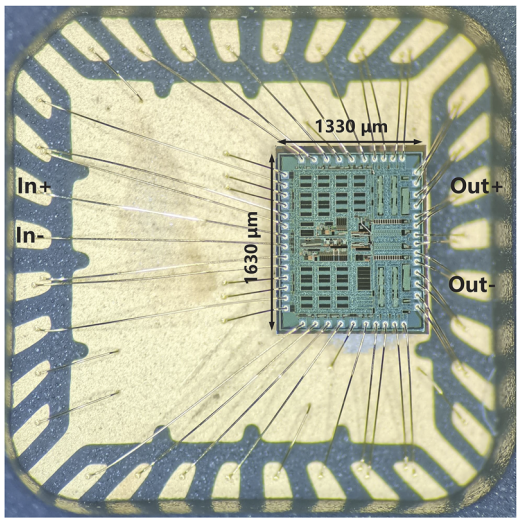


FIG. 8. Chip package.

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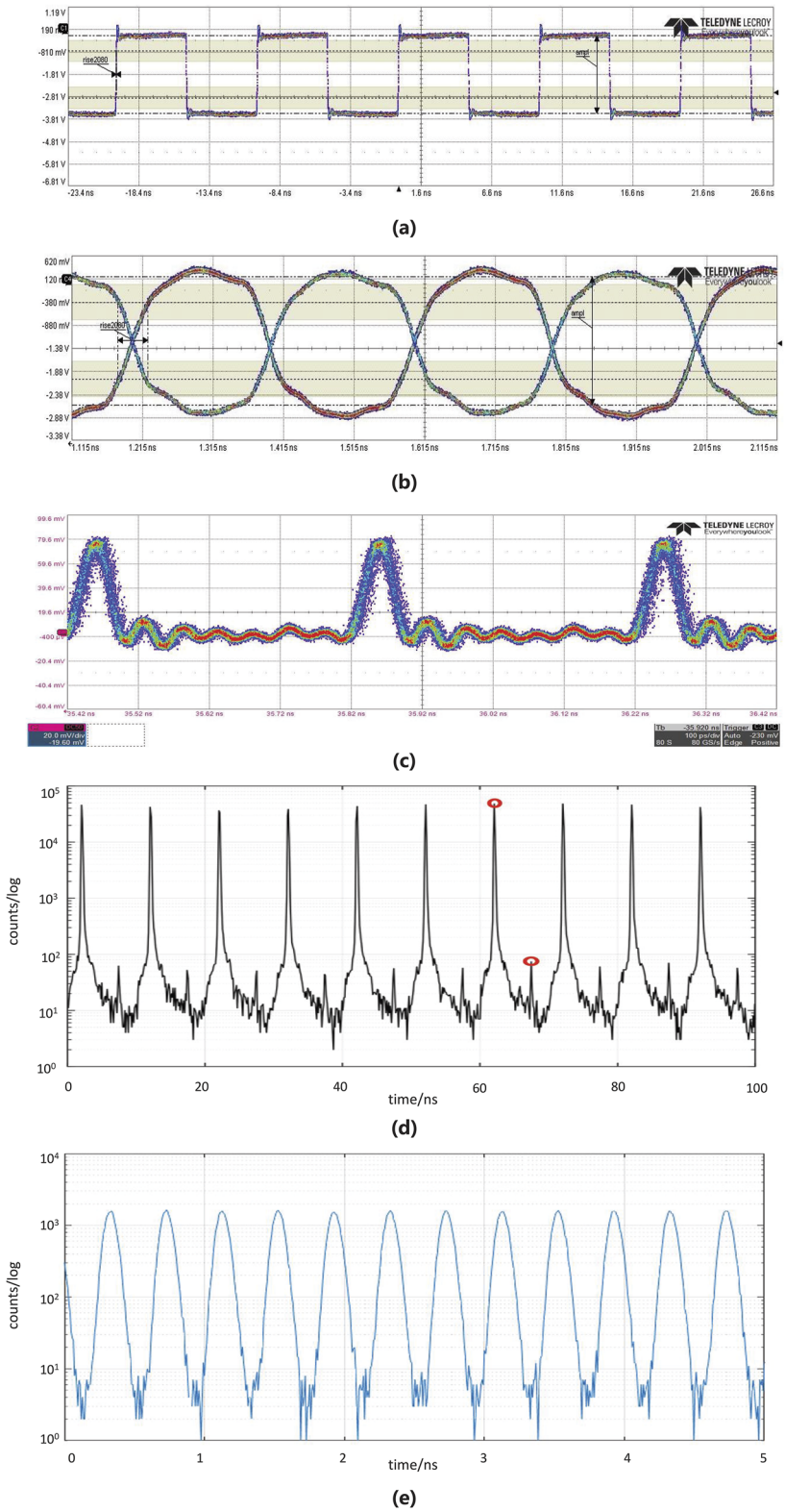


FIG. 9. Test diagram. (a) Single-ended output electrical signal at 100 MHz. (b) Output electrical signal at 2.5 GHz. (c) Optical signal diagram. (d) Optical signal diagram tested by SPD in previous version. (e) Optical signal diagram tested by SPD.

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Both the driver's circuitry characterizations and the LD's optical characterizations by applying the driver are presented. First, we connected the differential output signal of the driver directly to the oscilloscope (Tektronix DPO7354C). The input signal was generated using a pattern generator (Keysight 81134A). Figure 9(a) shows single-ended electrical diagrams of the driver circuit at 100 MHz with a voltage amplitude of 3.5 V. The rise and fall time (20%–80%) is ~46 ps, and the bandwidth is ~5 GHz. Figure 9(b) shows test diagrams of the laser driver outputting an electrical signal with a pulse-width of 200 ps at repetition frequencies of 2.5 GHz; simultaneously, the internal modulation current is set to a typical value of 100 mA. The laser's optical signal travels down the optical fiber to the fiber-optic detector (NewFocus model 1444), where it is transformed into an electrical signal and shown on the oscilloscope. Figure 9(c) depicts the optical signal of a laser driven by an electrical signal with a 200 ps pulse-width. The optical signal's pulse-width is ~50 ps, which is narrower than the electrical signal's pulse-width. The realistic pulse-width of the optical signal is narrower due to the bandwidth restrictions of the oscilloscope and fiber-optic detector.

The optical signal's extinction ratio is important since it directly impacts the QKD systems' coding rate. The ratio between the peak pulse power and the maximum power of the undamaged background signal is known as the extinction ratio of the optical pulse signal.[31] The optical pulse's extinction ratio represents the light intensity. The ratio of the maximum light intensity to the minimum light intensity of the corresponding light pulse exceeds 100 times for an extinction ratio requirement greater than 20 dB. The optical pulse extinction ratio value cannot be precisely determined on the oscilloscope due to the interference from the fiber-optic detector and oscilloscope noise. In most cases, the laser's optical pulse signal needs to be attenuated and then detected by a single-photon detector (SPD); then, the number of photons is counted by the time tagger to measure the precise extinction ratio. Figure 9(d) depicts the extinction ratio of the 1550-nm DFB laser using the circuit driver in CMOS technology.[16] The reflection peaks marked with red circles can be seen in the diagram. Reflective peaks deteriorate the extinction ratio making it impossible to meet the requirement at high frequencies. Through our improvements, the extinction ratio of the 1550-nm DFB laser can reach 23 dB, which is shown in Fig. 9(e), satisfying the requirement.

Overall, we have finished testing and measuring the driver chip. The maximum clock frequency of the driver was 2.5 GHz. The pulse-width of the output current signal can be adjusted up to 100 ps. The internal current amplitude is also adjustable up to 140 mA. The output current amplitude can be up to ~100 mA, considering that the equivalent load resistance of LD is ~21 Ω at high speed application. In terms of functionality and performance, the driver meets the requirements.

IV. CONCLUSION

We present a circuit for driving a light source in a QKD system. The chip is manufactured in 0.18 μm SiGe BiCMOS technology, and the chip size is 1633 × 1330 μm^2. The driver circuit can drive a 1550-nm DFB LD operating as a weak coherent light source for QKD experiments. The circuit can operate at frequencies up to 2.5 GHz. The output current of the driver circuit can reach 100 mA when driving an LD whose input equivalent resistance is ~21 Ω. The extinction ratio of the optical signals produced by the 1550-nm DFB LD reaches 23 dB at an operating frequency of 2.5 GHz. Co-packaging of integrated photonics and electronics is a solution for miniaturization of the QKD system. We intend to co-package the integrated photonics and electronics to improve the integration of the QKD device. This work completes the laser driver of the integrated electronics.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Yulong Zhu: Conceptualization (lead); Data curation (lead); Investigation (lead); Methodology (lead); Writing – original draft (lead); Writing – review & editing (lead). **Xinzhe Wang**: Project administration (lead); Validation (equal). **Chenxi Zhu**: Methodology (equal). **Zhaoyuan Chen**: Investigation (equal). **Zhisheng Huang**: Validation (equal). **Zhanhong Jin**: Investigation (equal). **Yang Li**: Conceptualization (equal). **Futian Liang**: Resources (lead); Supervision (lead); Writing – review & editing (equal). **Shengkai Liao**: Funding acquisition (equal); Supervision (equal). **Chengzhi Peng**: Funding acquisition (equal); Supervision (equal). **Ge Jin**: Funding acquisition (equal); Supervision (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

REFERENCES

[1]C. H. Bennett, "Quantum cryptography: Public key distribution and coin tossing," in *Proc. of IEEE International Conference on Computers* (IEEE, 1984).
[2]C. H. Bennett, F. Bessette, G. Brassard, L. Salvail, and J. Smolin, "Experimental quantum cryptography," J. Cryptology **5**, 3–28 (1992).
[3]S.-K. Liao, W.-Q. Cai, W.-Y. Liu *et al.*, "Satellite-to-ground quantum key distribution," Nature **549**, 43–47 (2017).
[4]Y.-A. Chen, Q. Zhang, T.-Y. Chen, W.-Q. Cai, S.-K. Liao, J. Zhang, K. Chen, J. Yin, J.-G. Ren, Z. Chen, S.-L. Han, Q. Yu, K. Liang, F. Zhou, X. Yuan, M.-S. Zhao, T.-Y. Wang, X. Jiang, L. Zhang, W.-Y. Liu, Y. Li, Q. Shen, Y. Cao, C.-Y. Lu, R. Shu, J.-Y. Wang, L. Li, N.-L. Liu, F. Xu, X.-B. Wang, C.-Z. Peng, and J.-W. Pan, "An integrated space-to-ground quantum communication network over 4,600 kilometres," Nature **589**, 214–219 (2021).
[5]H.-K. Lo, X. Ma, and K. Chen, "Decoy state quantum key distribution," Phys. Rev. Lett. **94**, 230504 (2005).

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[6]H.-K. Lo, M. Curty, and B. Qi, "Measurement-device-independent quantum key distribution," Phys. Rev. Lett. **108**, 130503 (2012).
[7]M. Lucamarini, Z. L. Yuan, J. F. Dynes, and A. J. Shields, "Overcoming the rate–distance limit of quantum key distribution without quantum repeaters," Nature **557**, 400 (2018).
[8]V. Scarani, H. Bechmann-Pasquinucci, N. J. Cerf, M. Dušek, N. Lütkenhaus, and M. Peev, "The security of practical quantum key distribution," Rev. Mod. Phys. **81**, 1301–1350 (2009).
[9]S. Sajeed, P. Chaiwongkhot, A. Huang, H. Qin, V. Egorov, A. Kozubov, A. Gaidash, V. Chistiakov, A. Vasiliev, A. Gleim, and V. Makarov, "An approach for security evaluation and certification of a complete quantum communication system," Sci. Rep. **11**, 5110 (2021).
[10]J.-Y. Wang, B. Yang, S.-K. Liao, L. Zhang, Q. Shen, X.-F. Hu, J.-C. Wu, S.-J. Yang, H. Jiang, Y.-L. Tang *et al.*, "Direct and full-scale experimental verifications towards ground–satellite quantum key distribution," Nat. Photonics **7**, 387–393 (2013).
[11]Y. Cao, Y.-H. Li, K.-X. Yang, Y.-F. Jiang, S.-L. Li, X.-L. Hu, M. Abulizi, C.-L. Li, W. Zhang, Q.-C. Sun *et al.*, "Long-distance free-space measurement-device-independent quantum key distribution," Phys. Rev. Lett. **125**, 260503 (2020).
[12]C.-X. Zhu, Z.-Y. Chen, Y. Li, X.-Z. Wang, C.-Z. Wang, Y.-L. Zhu, F.-T. Liang, W.-Q. Cai, G. Jin, S.-K. Liao, and C.-Z. Peng "Experimental quantum key distribution with integrated silicon photonics and electronics," Phys. Rev. Appl. **17**, 064034 (2022).
[13]C.-Z. Peng, J. Zhang, D. Yang, W.-B. Gao, H.-X. Ma, H. Yin, H.-P. Zeng, Y. Tao, X.-B. Wang, and J. W. Pan, "Experimental long-distance decoy-state quantum key distribution based on polarization encoding," Phys. Rev. Lett. **98**, 010505 (2007).
[14]E. Sinchenko, *Fibre Optic Distributed Corrosion Sensor* (Faculty of Engineering and Industrial Science, Melbourne, 2013).
[15]J.-P. Bourgoin, E. Meyer-Scott, B. L. Higgins, B. Helou, C. Erven, H. Hübel, B. Kumar, D. Hudson, I. D'Souza, R. Girard, R. Laflamme, and T. Jennewein, "A comprehensive design and performance analysis of low Earth orbit satellite quantum communication," New J. Phys. **15**, 023006 (2013).
[16]B. Feng, F. Liang, X. Wang, C. Zhu, Y. Zhu, and G. Jin, "A laser source driver with adjustable amplitude and pulse-width in 130-nm CMOS technology for quantum key distribution experiments," Rev. Sci. Instrum. **90**, 064704 (2019).
[17]X. Wang, F. Liang, B. Feng, C. Zhu, Y. Zhu, and G. Jin, "Integrated electronics in 130 nm CMOS process for quantum key distribution sender device," Rev. Sci. Instrum. **91**, 034701 (2020).
[18]A. Wahba, L. Cheng, and F. Lin, "A 15 Gbps-NRZ, 30 Gbps-PAM4, 120 mA laser diode driver implemented in 0.15-μm GaAs E-mode pHEMT technology," J. Semicond. **42**, 072401 (2021).
[19]S. Mandegaran and A. Hajimiri, "A breakdown voltage multiplier for high voltage swing drivers," IEEE J. Solid-State Circuits **42**(2), 302–312 (2007).
[20]S. Voinigescu, *High-Frequency Integrated Circuits* (Cambridge University Press, 2013).
[21]J. C. Cartledge and R. C. Srinivasan, "Extraction of DFB laser rate equation parameters for system simulation purposes," J. Lightwave Technol. **15**, 852–860 (1997).
[22]Y. L. Tang, H. L. Yin, X. Ma, C. Fung, Y. Liu, H. L. Yong, T. Y. Chen, C. Z. Peng, Z. B. Chen, and J. W. Pan, "Source attack of decoy-state quantum key distribution using phase information," Phys. Rev. A **88**, 5862–5868 (2013).
[23]T. Kobayashi, A. Tomita, and A. Okamoto, "Evaluation of the phase randomness of a light source in quantum key distribution systems with an attenuated laser," Phys. Rev. A **90**(3), 032320 (2014).
[24]R. Schmid, T. F. Meister, M. Rest, and H.-M. Rein, "SiGe driver circuit with high output amplitude operating up to 23 Gb/s," IEEE J. Solid-State Circuits **34**, 886–891 (1999).
[25]M. A. Oakley, U. S. Raghunathan, B. R. Wier, P. S. Chakraborty, and J. D. Cressler, "Large-signal reliability analysis of SiGe HBT cascode driver amplifiers," IEEE Trans. Electron Devices **62**, 1383–1389 (2015).
[26]H.-M. Rein, R. Schmid, P. Weger, T. Smith, T. Herzog, and R. Lachner, "A versatile Si-bipolar driver circuit with high output voltage swing for external and direct laser modulation in 10 Gb/s optical-fiber links," IEEE J. Solid-State Circuits **29**, 1014–1021 (1994).
[27]H.-M. Rein and M. Moller, "Design considerations for very-high-speed Si-bipolar IC's operating up to 50 Gb/s," IEEE J. Solid-State Circuits **31**, 1076–1090 (1996).
[28]M. Rickelt and H. M. Rein, "A novel transistor model for simulating avalanche-breakdown effects in Si bipolar circuits," IEEE J. Solid-State Circuits **37**, 1184–1197 (2003).
[29]H. Hettrich and M. Möller, "Design considerations for a 11.3 Gbit/s SiGe bipolar driver array with a 5×6 V_{pp} chip-to-chip bondwire output to an MZM PIC," IEEE J. Solid-State Circuits **51**, 2006–2014 (2016).
[30]H. Hettrich and M. Möller, "Linear low-power 13 GHz SiGe-bipolar modulator driver with 7 Vpp differential output voltage swing and on-chip bias tee," in *Bipolar/Bicmos Circuits and Technology Meeting* (IEEE, 2014).
[31]M. L. Nielsen, B.-E. Olsson, and D. J. Blumenthal, "Pulse extinction ratio improvement using SPM in an SOA for OTDM systems applications," IEEE Photonics Technol. Lett. **14**, 245–247 (2002).

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