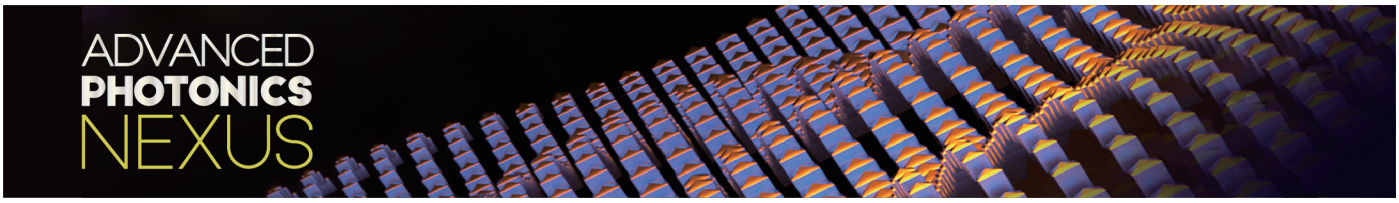
Research Article



Hybrid optoelectronic-integrated module design for quantum communication

Zhao-Yuan Chen, Yan-Fei Liu,* Xiao-Sheng Si, Hao Zheng, Tian-Mei Li, Lei Feng, and Hǎo Zheng
Rocket Force University of Engineering, Xi'an, China

Abstract. Quantum key distribution (QKD) technology is progressively transitioning from experimental research to industrial development. The development of highly integrated and stable QKD modules has thus emerged as a new research direction. Current integrated QKD research primarily focuses on the integration of optical systems, with relatively few studies addressing optoelectronic co-integration. Due to the more stringent demands of QKD systems on driving signal amplitude, noise, and bandwidth, the driving electronics become more complex and power-intensive, making it difficult to achieve the level of optoelectronic integration seen in classical optical communication systems. We propose a hybrid optoelectronic integrating scheme for QKD modules based on chip-on-board technology, which co-packages the QKD-encoding photonic chip and its required electronic driver chips within a compact, centimeter-scale module. By optimizing the layout structure, incorporating thermal management, and implementing active temperature control, the module temperature can be stabilized within a set range. Simulation and experimental results demonstrate that the module has a total power consumption of 7.69 W and can maintain a stable temperature of 45°C for extended periods when the thermoelectric cooler is active. This effectively ensures the stable operation of the photonic chip and supports long-term QKD functionality, thereby providing technical support for advancing hybrid optoelectronic integrated QKD systems.

Keywords: quantum communication; hybrid packaging; chip-on-board; thermal management.

Received Nov. 3, 2025; revised manuscript received Dec. 29, 2025; accepted for publication Dec. 31, 2025; published online Jan. 24, 2026.

© The Authors. Published by SPIE and CLP under a Creative Commons Attribution 4.0 International License. Distribution or reproduction of this work in whole or in part requires full attribution of the original publication, including its DOI.

[DOI: 10.1117/1.APN.5.3.036001]

1 Introduction

Quantum key distribution (QKD) harnesses fundamental quantum mechanical principles to provide security in key exchange, positioning it as a pivotal technology for future secure communications in an era of rising quantum computing threats.[1–3] Recent breakthroughs have demonstrated its practical potential: microsatellite-based QKD, exemplified by China's Jinan-1 mission, has achieved real-time key distribution between microsatellites and the ground;[4] high-speed systems now support key rates exceeding 110 Mbps within a 10-km fiber distance;[5] and multi-node quantum networks, such as the Beijing–Shanghai backbone, are already operational.[6] Despite these advances, the transition of QKD from laboratory demonstrations to broad industrial application remains hindered by its reliance on bulky, discrete optical, and electronic components, which results in high unit costs and limited operational stability.

This drive toward industrialization emphasizes reliability, cost-effectiveness, and scalable fabrication—criteria for which integrated photonics technology is particularly well-suited.[7,8] Photonic integrated circuits (PICs) offer miniaturization, reduced power consumption, and compatibility with semiconductor processes, making them an ideal platform for future quantum communication systems.[9,10] Significant progress has been made in developing QKD PICs, such as transmitters for various protocols[11–20] and receivers for different decoding types.[13,21–28] Most of these studies have focused on the integration of optical components within QKD terminals, such as integrated encoder and decoder PICs. However, a fully functional QKD transmitter is composed of a light source, an encoder, a decoder, and the peripheral driving circuits to realize quantum state encoding and transmission (or reception and decoding). Although PICs have replaced discrete and cumbersome

*Address all correspondence to Yan-Fei Liu, bbmcu@126.com

fiber-optic and electro-optic components, their operation still relies on corresponding driving and control circuits. Research on optoelectronic interconnects and high-density integration for QKD systems is still in its early stages. For instance, Sax et al. have made an attempt to integrate the QKD PIC encoder and the electrical driver together using a special process.[29] In addition, Hajomer et al. successfully integrated the photo-diode (PD) at the receiving end and the TIA onto a small module.[25] All these works have made some attempts at the optoelectronic integration of part of QKD systems, and to the best of our knowledge, no such fully integrated optoelectronic solution for QKD has been reported. This has consequently led to the physical size of the electronic driving systems becoming a primary factor limiting the further integration of QKD terminals.

It is noteworthy that the classical optical communications industry has made significant strides in the research of hybrid optoelectronic integrated modules, providing an experienced roadmap for the industrialization of QKD technology. Although QKD and classical optical communications can adopt similar design approaches for some technical implementations, there remain considerable differences in their specific functional requirements and performance metrics. On the one hand, their functional requirements for driving signals differ. Classical optical communications typically require only binary amplitude levels for modulation, whereas QKD necessitates driving signals with multiple distinct voltage amplitudes to encode several different quantum states. This requirement substantially increases the complexity of driving circuit design. Therefore, in previous QKD demonstration experiments, most systems still relied on arbitrary waveform generators (AWGs) or custom-designed, specialized PCB circuits to drive the optical chips. Constrained by the physical size of these driving circuits, the integration advantage of PICs is compromised. On the other hand, their performance requirements for the driving signal are different. Taking intensity modulation in optical communications and decoy-state preparation as an example, the depth of intensity modulation in classical optical communications typically requires only 3 to 10 dB,[30–32] whereas QKD applications demand an extinction ratio exceeding 20 dB for intensity modulation. Consequently, QKD applications impose stricter requirements on the electrical signal amplitude and noise characteristics of driving circuits, which also results in higher power consumption.[33] For instance, in some integrated photonic chip-based QKD experiments, the half-wave voltage of electro-optic modulators is around 3 to 5 V.[12,13,34–36] However, actual quantum state preparation requires modulation up to a phase of $3\pi/2$, necessitating even higher driving voltages and additional radio-frequency (RF) amplification circuits, further increasing the power consumption. PICs are typically highly sensitive to temperature variations. In compact modules, heat accumulation from power dissipation can significantly compromise the operational stability of these photonic components. Therefore, implementing effective thermal management is crucial in hybrid optoelectronic-integrated modules.

Due to the aforementioned reasons, achieving highly integrated modules for QKD—similar to those in classical optical communication transmitters—presents significant challenges in electronic design, optoelectronic co-packaging, and thermal management. In this work, we present a hybrid optoelectronic integrated QKD transmitter scheme for the decoy-state BB84 protocol through chip-on-board (COB) technology. This approach integrates a QKD PIC, along with its necessary driver electronic-integrated chips (EICs) and RF amplifier chips into a compact, centimeter-scale module utilizing direct wire bonding. Through proper thermal design and temperature control, the operating temperature of the entire module can be maintained within an acceptable range. This work offers a new technical pathway for the further integration of QKD systems.

2 Methodology

In this section, we introduce the design methodology of the integrated module. The structure of the hybrid optoelectronic integrated QKD transmitter is illustrated in Fig. 1. The core components of the module consist of a laser diode (LD) chip, a QKD encoder PIC, and their associated driver electronic-integrated chips (EICs). A clock signal data1 with a specific frequency is input into the laser driver chip (LSD). The LSD converts this signal into a driving current, which gain-switches the LD to generate weak coherent pulses (WCPs). The WCPs are then injected into the QKD PIC via a fiber array (FA). Meanwhile, the two-channel random data signal (data2) is fed into the modulator driver chip (MDC). MDC1 converts this signal into a three-level pulse amplitude modulation (PAM-3) signal, which is amplified by an RF amplifier before being applied to the intensity modulator (IM) on the QKD PIC to modulate the intensity of the optical pulses. Similarly, the three-channel random data signal (data3) is input to MDC2. MDC2 converts it into a PAM-4 signal. After amplification by an RF amplifier, this signal drives the polarization modulator (POM) on the QKD PIC to encode polarization information onto the optical pulses. The encoded qubits are then emitted via the FA and sent to the receiver. The QKD encoder PIC and its driver electronics are hybrid integrated using COB technology. All chips are mounted on a compact PCB substrate and interconnected through direct wire bonding, achieving both higher integration density and improved signal transmission quality.

2.1 QKD PIC

The polarization-encoding decoy-state BB84 QKD protocol is adopted. Therefore, the QKD PIC integrates an IM and a POM, as illustrated in Fig. 2(a), to prepare decoy and polarization states. Both the IM and POM are modulators based on the Mach-Zehnder interferometer (MZI) structure. Laser pulses are coupled into the PIC via a grating coupler (GC) and then enter the IM. Pulses are first split by a multimode interferometer (MMI) into two beams that propagate through the two interferometer arms. A heater provides a fixed phase bias, setting the MZI at its initial destructive interference state. The high-speed modulator then applies a modulation signal, introducing a phase difference between

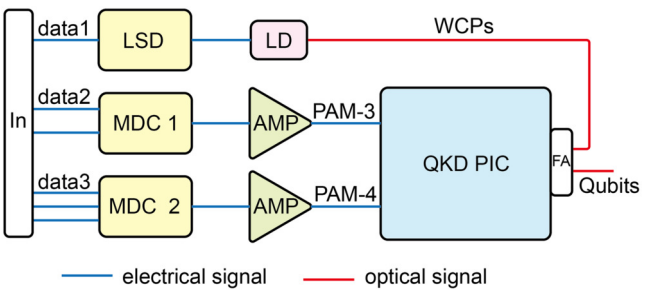


Fig. 1 Schematic of the QKD transmitter module. The entire module fulfills the function of QKD encoding and transmission.

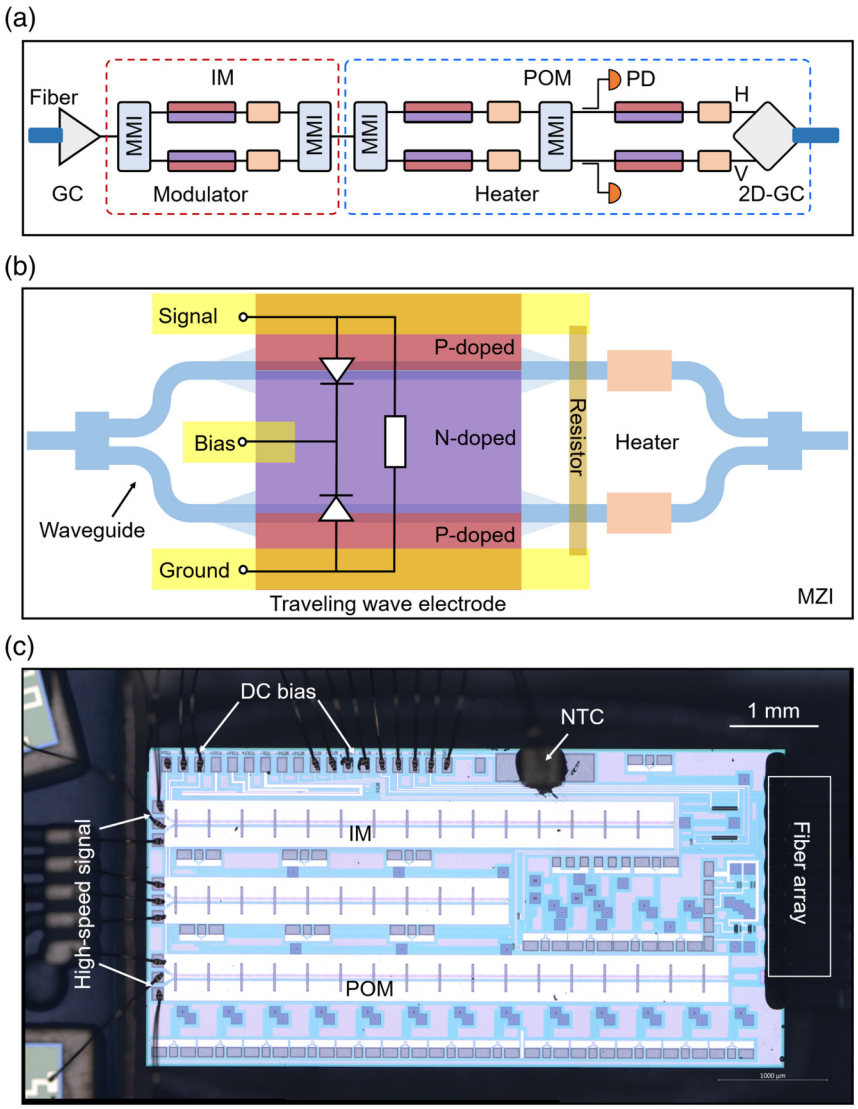


Fig. 2 (a) Schematic diagram of the PIC optical circuit. The optical signal is coupled into the chip via a grating coupler (GC). It is then modulated by an IM and a POM before being output through a two-dimensional grating coupler (2D-GC). (b) Schematic diagram of the equivalent circuit of the MZI. The MZI consists of two PN junctions placed opposite each other in a push-pull structure. (c) A photo of the QKD PIC. The high-speed and the DC signal interface are located on the left and top of the chip, respectively, and an NTC thermistor is placed on the upper right of the chip.

the two arms. This modulates the output pulses into decoy-state signals with different intensities. Subsequently, the modulated decoy-state pulses enter the POM, which features a two-stage MZI configuration. The first stage functions as a tunable beam splitter, dividing the input pulse into two beams ($\alpha|H\rangle$ and $\beta|V\rangle$) according to the applied electrical signal, which are then fed into the second stage. Two PDs are integrated after the first stage to monitor the optical power. The second MZI stage modulates the relative phase difference between the H and V beams. Finally, the modulated H and V beams are combined at a two-dimensional grating coupler, generating the desired modulated polarization state ($\alpha|H\rangle + \beta|V\rangle e^{i\phi}$). The waveguide is designed as a standard single-mode silicon waveguide with a width of 500 nm and a thickness of 220 nm. The bend radius at the waveguide connections is 15 μm. The overall optical loss, including the grating couplers, is ~32 dB.

The MZI incorporates a high-speed modulator (about 20 GHz bandwidth) based on the plasma dispersion effect and a phase shifter based on the thermo-optic effect. The schematic of the MZI structure is presented in Fig. 2(b). P-type doping is applied to the outer regions of the two arms of the MZI, whereas N-type doping is implemented on the inner regions, forming two opposing PN junctions at the center of the waveguides. The P-doped regions are connected to two traveling-wave electrodes, respectively, and the N-doped region is connected to a bias electrode. A 50-ohm resistor is placed between the two traveling-wave electrodes to achieve better impedance matching. Heaters are integrated onto the waveguides of both interferometer arms to provide a phase bias for the MZI. The optical signal is split by an MMI into two beams that propagate through the two interferometer arms. The phase in the lower arm is fixed, whereas the phase in the upper arm is modulated by an electrical signal.

This configuration introduces a relative phase difference between the two arms. The lengths of the MZI in IM and POM are 5 and 5.5 mm, respectively, with a half-wave voltage of ∼3.5 V. The MZI modulator operates in a reverse-biased push-pull configuration, where the PN junction functions as a carrier-depletion modulator to achieve higher modulation bandwidth.

This PIC was fabricated through a multi-project wafer (MPW) process on a 180-nm silicon-on-insulator (SOI) platform in CompoundTek for cost-effectiveness. The QKD PIC measures 5.80 mm × 2.95 mm, and the chip wire bonding is shown in Fig. 2(c). The driving signals for the modulators are applied through the high-speed GSG (ground-signal-ground) electrodes located on the left side of the chip. The two lines indicated in the figure correspond to the connections between the QKD PIC's IM and POM and their respective driver chips. The DC bias electrodes are positioned at the top of the chip, providing functions including MZI modulator biasing, phase shifter biasing, and PD monitoring. A negative temperature coefficient (NTC) thermistor is placed at the upper right section to monitor the chip temperature and provide feedback to the temperature control module for thermal regulation. An FA is mounted on the right side of the chip using an index-matching adhesive to facilitate the coupling of optical signals into and out of the chip. The coupling loss between the grating couplers and the FA is ∼3.5 dB.

2.2 Driver EIC

We employed a custom-designed MDC and a commercially available RF amplifier chip to form the driving circuit for the QKD PIC, with a simplified schematic diagram illustrated in Fig. 3(a). The MDC requires three supply voltages: VDD, VCC, and VEE. Under the control of the amplitude adjustment signal (V-set) and the pulse width adjustment signal (PWC), the MDC converts the input data signals into corresponding driving signals, which are then output to the amplifier. The amplifier has a maximum gain of 19 dB and a bandwidth covering DC to 15 GHz. The amplifier requires two supply voltages, denoted as VGG and ACG. By adjusting the amplifier gain, the driving signals are amplified to an appropriate level and subsequently fed into the MZI modulator for quantum state preparation.

Figure 3(b) shows the wire bonding of the MDC, where three-channel data signals are fed into the chip from the left side and converted into PAM-4 driving signals output from the right. The amplitude of the output signals can be controlled via several V-set signals, enabling arbitrary adjustment of each amplitude to meet the requirements of specific quantum state preparation. Other bonding wires are used for functions such as power supply and pulse width adjustment. Figure 3(c) is a wire bonding photograph of the amplifier. The amplified driving signals are directly delivered to the POM on the PIC via bonding wires. The length of these wires is minimized to reduce the effects of impedance mismatch.

2.3 Packaging Design

The MDC and amplifier exhibit power consumption of ∼1.7 and 1 W, respectively. The thermal power consumption of the QKD PIC is around 2.5 W. Because one QKD encoding module requires two sets of such driving circuits, the total power consumption of the module reaches around 7 to 8 W. The QKD PIC, fabricated on a silicon platform, possesses a large thermo-optic coefficient. Without effective thermal management, this would lead to significant phase drift. Furthermore, both the MDC and amplifier require multiple supply voltages and control signals, resulting in complex routing within a constrained footprint. Special attention must be paid to the high-speed driving signals, which require isolation and filtering to mitigate signal crosstalk. In addition, these chips are manufactured using different fabrication processes, leading to variations in die thickness. To enhance signal transmission performance and mechanical robustness, the chips must be planarized to the same level. To address these issues, we propose a COB packaging scheme in which the dies are mounted directly onto a PCB. Interconnection between chips, as well as signal input and control, is achieved through a hybrid approach utilizing both wire bonding and PCB traces.

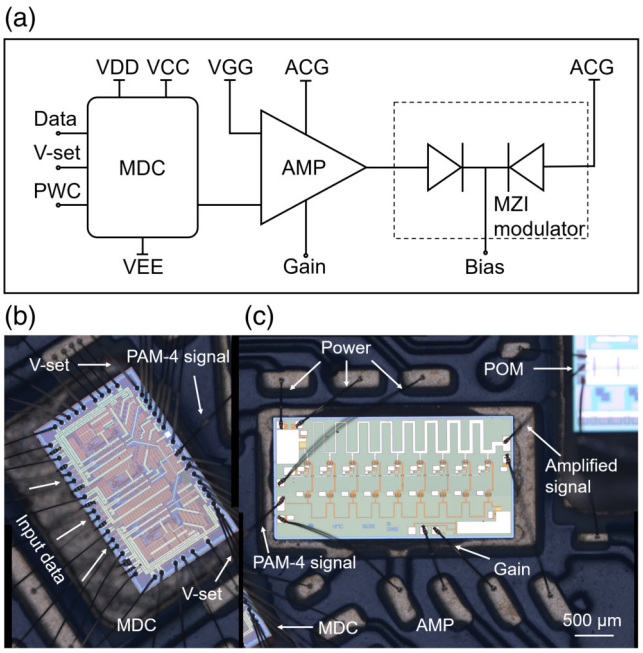


Fig. 3 (a) Schematic diagram of chip connection and power supply. Under the control of the V-set and PWC configuration signals, the MDC converts the input data signal into a drive signal, which is then amplified by an AMP and input into the MZI modulator. (b), (c) Photos of MDC and AMP chip binding wires. AMP, amplifier.

First, as illustrated in Fig. 4, cavities with specific depths were pre-fabricated on the PCB according to the thickness of each die. The dies were then mounted into their respective cavities, ensuring co-planarity of all top surfaces. Then, wire bonding is employed to achieve signal interconnection between the chips. The PIC utilizes an FA for the input and output coupling of optical signals. A metal pad is incorporated at the bottom of each cavity. These pads serve dual purposes: providing power or ground connections to the chip, as well as facilitating heat dissipation. The top-side pads are connected to corresponding pads on the rear side of the PCB through vias. The heat is then transferred to a thermoelectric cooler (TEC) for active cooling. TEC controls the temperature of the entire module within the set range through the feedback of the NTC thermistor.

Figure 5 illustrates the PCB layout design. Figure 5(a) is the top side of the PCB. The five larger pads in the central area correspond to two MDCs, two AMPs, and one QKD PIC. The pads

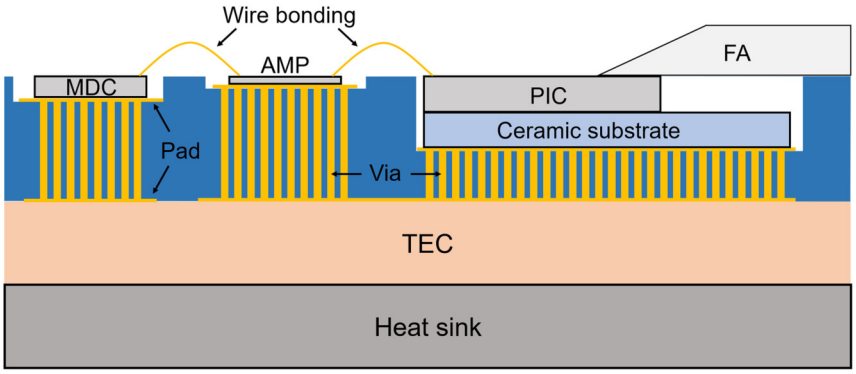


Fig. 4 Cross-section view of the COB module. Each chip is placed in a cavity of the corresponding depth and connected to the back heat-dissipation structure through vias. The PIC is placed on a ceramic substrate to meet the requirements of heat dissipation and bandwidth.

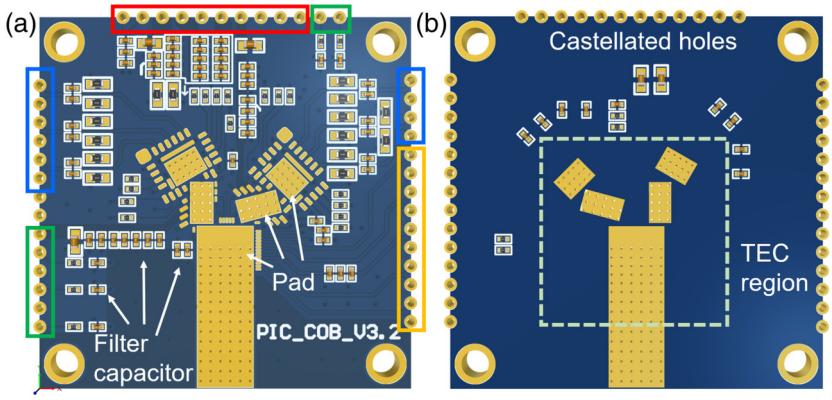


Fig. 5 PCB layout design of the COB module. (a) The chip and resistor components are placed on the top side. To minimize the interconnect distance and reduce the bonding wire length, the chip pads have been rearranged into the layout shown in the figure. (b) Space for the TEC is reserved on the bottom side.

for the MDCs are connected to the VEE, whereas those for the AMPs and PIC are connected to ground. Castellated holes are arranged along three edges of the PCB to facilitate module power supply, signal input, and control signals. The castellated holes within the red box serve as the power input interfaces for the chips. Data signals for polarization and intensity modulation are fed into the two MDCs via the castellated holes marked by the blue box. Amplitude control signals for the MDCs and gain control signals for the AMPs are supplied externally through the castellated holes in the green box. The castellated holes within the yellow box are dedicated to monitoring the PD current, reading thermistor values, and controlling the phase shifters on the PIC. Multiple filter capacitors are placed around the AMPs and PIC to reduce high-frequency driving noise. Figure 5(b) is the bottom side of the PCB. Each chip is connected to thermal pads on the rear side through vias. A TEC is attached to this side to regulate the temperature of the entire module.

The entire module measures only 3 cm × 3 cm, comparable to the size of a coin, as shown in Fig. 6. The COB module is mounted on the control board, which supplies power, data signals, and configuration signals. A cutout was designed on the control board directly beneath the COB module to accommodate the mounting of the TEC and heat sink. This hybrid packaging approach enables ultra-compact module size while maintaining

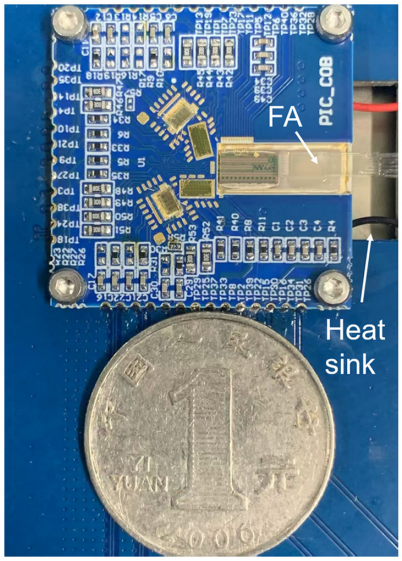


Fig. 6 Photo of the COB module installation. The COB module is first mechanically fixed to the system control board through screws and then electrically connected through castellated holes. The TEC and heat sink are attached to the back of the module.

signal integrity by avoiding parasitic losses typical of discrete interconnects like bonding wires and PCB traces.

3 Results

We first modeled the entire module structure to simulate the thermal distribution under various operational conditions. The PCB engineering files were imported into the simulation software, with the ambient temperature set to 20°C and all chip power consumptions configured to their operational levels. The thermal simulation results under different TEC current operating conditions are presented in Fig. 7. The worst-case power consumption was evaluated by operating the modulator under DC drive conditions, resulting in a module power consumption of 7.69 W. When the TEC was disabled as depicted in Fig. 7(a), the module temperature exceeded 59°C, with the amplifier chip and PIC recording temperatures of 75.1°C and 73.2°C, respectively. As the TEC current increased from 0 to 0.8 A, the module temperature demonstrated a decreasing trend. However, when the current exceeded 0.8 A, further increases led to a temperature rise. The simulated PIC temperatures under different TEC currents, along with the corresponding TEC cooling and heating power, were compiled in Fig. 8. The simulation results indicate that the cooling capacity of the TEC increases approximately linearly with rising current. However, the associated heating power grows at a faster rate, particularly when the current exceeds 0.8 A, where a rapid increase in heating power leads to heat transfer from the hot side to the cold side, thereby diminishing the TEC's cooling effect. At ~0.8 A, the PIC temperature can be reduced to 43.7°C.

Subsequently, we conducted experimental validation of the module's thermal stability. Initially, with the TEC disabled, we employed a thermal imaging camera to monitor the temperature rise during operation, with the results presented in Figs. 9(a)–9(l). At the beginning of the experiment, the module was at room temperature. Upon power activation, it began heating up rapidly. Within merely 1 min, the overall module temperature rose above 50°C, with the peak temperature reaching 65.6°C. The module continued to heat up gradually in the following minutes and after 10 min, the maximum temperature stabilized at 72.7°C. Throughout this process, the feedback temperature from the thermistor on the PIC is shown as the blue curve in Fig. 10. After allowing the module to return to room temperature, the temperature of the PIC was maintained at 45°C using a PID control algorithm. The temperature measurement results of the module with TEC activated are presented in Figs. 9(m)–9(p), whereas the corresponding PIC temperature recorded by the thermistor is shown as the red curve in Fig. 10. The experimental results

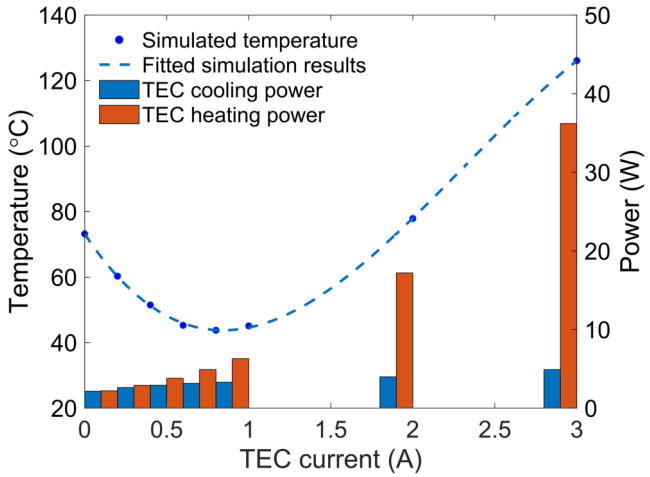


Fig. 8 Simulated PIC temperature (dashed line and data points) and TEC cooling/heating power (columns) versus TEC current.

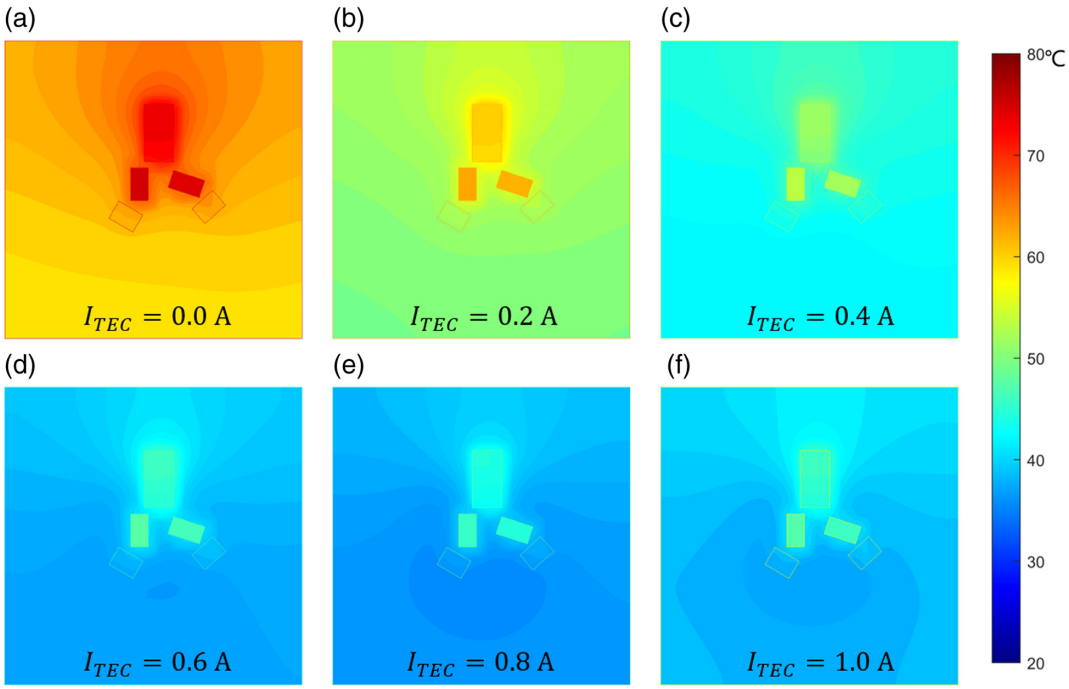


Fig. 7 (a)–(f) Simulated thermal distributions with different TEC currents. The colors in the figure represent different temperatures, with color bar scales from 20°C to 80°C.

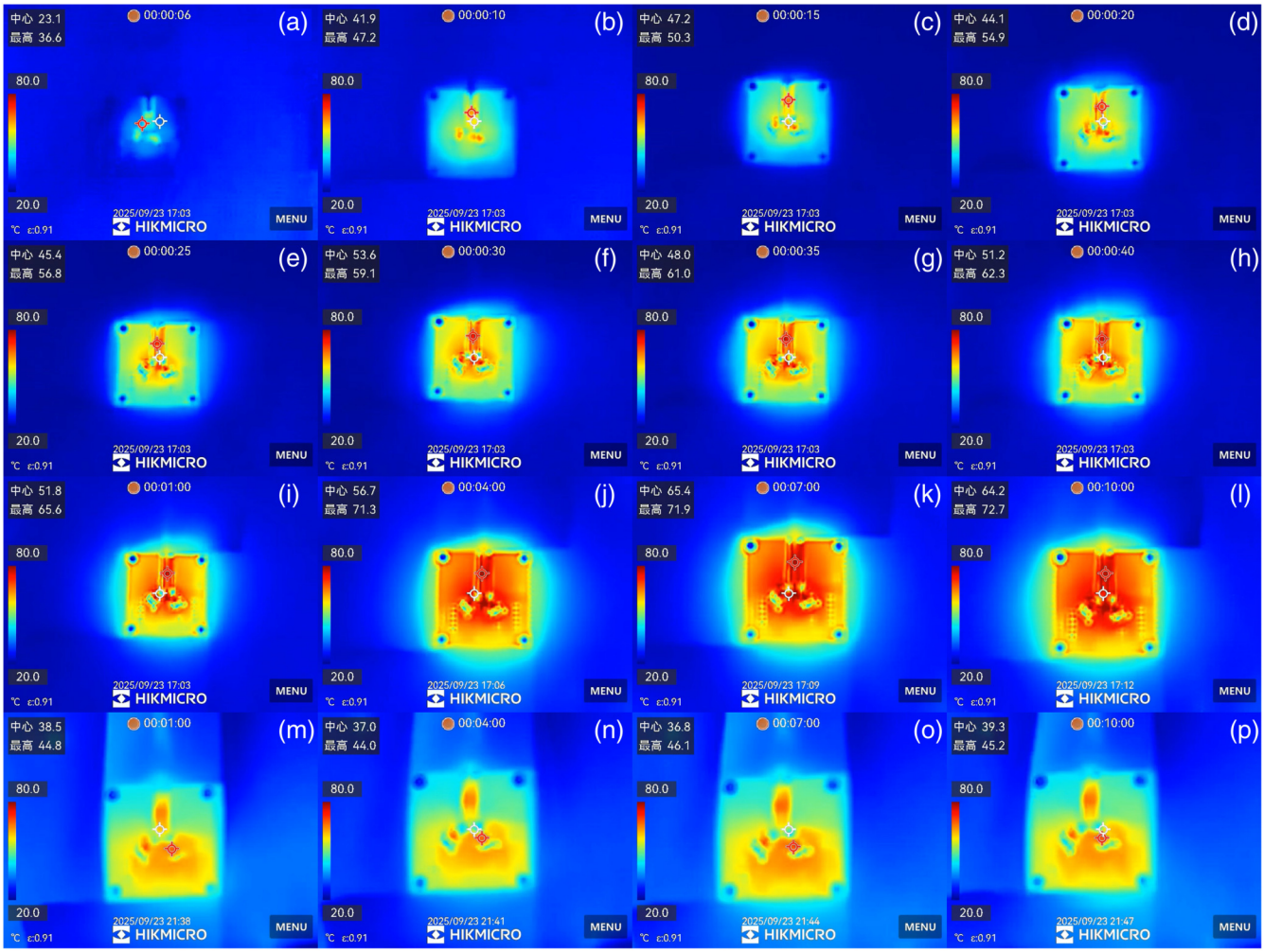


Fig. 9 Thermal imaging photos of the module during operation. Panels (a)–(l) represent the temperature when TEC is off, and panels (m)–(p) represent the temperature when TEC is on. The color bars represent the temperature in Celsius degrees, ranging from 20°C to 80°C.

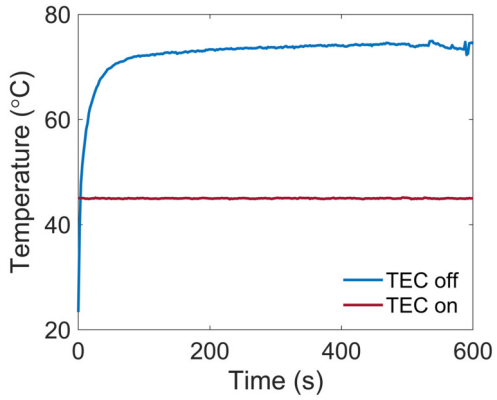


Fig. 10 Read temperatures of the NTC thermistor in different states. The blue and red data indicate TEC off and on, respectively.

demonstrate that the PIC temperature can be effectively maintained near the setpoint when the TEC is activated.

After hybrid integration, the driving signals are directly fed into the PIC, making them inaccessible for direct measurement. Therefore, we first characterized the signal properties of the discrete packaged MDC and RF amplifier chips to evaluate the optoelectronic characteristics. The output PAM-4 signals measured at clock rates of 1.25 and 2.5 GHz are shown in Fig. 11. Figures 11(a) and 11(b) respectively show the direct output signal from the MDC and the amplified signal after passing through the RF amplifier under a 1.25-GHz clock rate. The rise time of the MDC signal from 20% to 80% is about 50 ps. The amplified signal achieves a maximum amplitude exceeding 6 V. The signal demonstrates good integrity, satisfying both the speed and amplitude requirements for precise quantum state preparation. At a clock rate of 2.5 GHz, both the rise time of the MDC signal and the amplitude of the amplified signal show no significant degradation. However, after amplification, the rise time of the second and third levels becomes slower, resulting in deteriorated signal integrity. This effect may manifest in the optical modulation as a corresponding degradation in the extinction ratio. We conducted intensity modulation and polarization modulation tests under different packaging. At clock rates of 1.25 and 2.5 GHz, respectively, pseudo-random bit sequence data was fed into the MDC chip. The amplified signals were then used to drive the IM and POM on the PIC. Finally, the

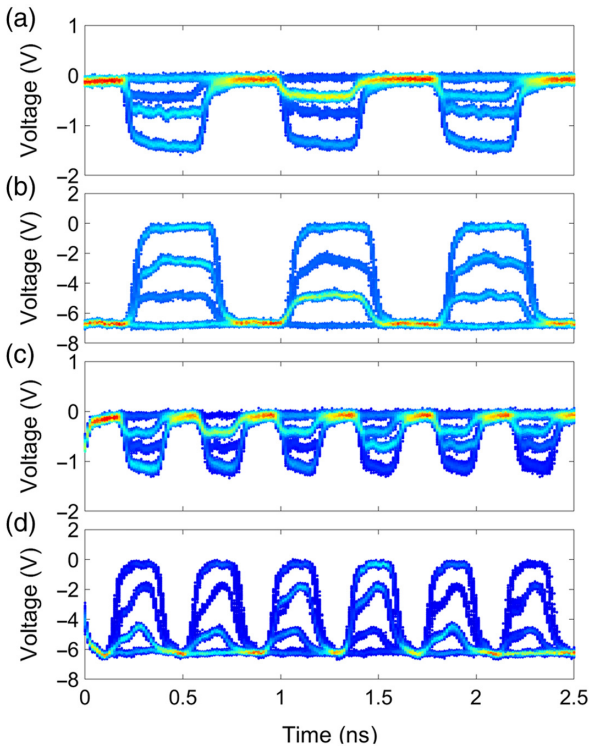


Fig. 11 Output signals of discrete packaged MDC and RF amplifier chips. Panel (a) is the MDC output signal at 1.25 GHz, and panel (b) is its amplified signal. Panels (c) and (d) represent these signals at 2.5 GHz. A 36-GHz-bandwidth oscilloscope operating at 80 GSa/s is used for data acquisition. The data points in the figure are displayed using the oscilloscope persistence effect.

Table 1 Average modulation extinction ratio.

Clock rate		1.25 GHz (dB)	2.5 GHz (dB)
Discrete packaging	IM	24.24	19.40
	POM	25.45	22.33
Hybrid packaging	IM	25.18	20.80
	POM	27.52	24.37

average modulation extinction ratios were measured, and the results were summarized in Table 1. At 1.25 GHz, the hybrid integrated module demonstrates extinction ratio improvements of 0.94 dB for intensity modulation and 2.07 dB for polarization modulation, respectively. At 2.5 GHz, the corresponding improvements are 1.40 and 2.04 dB. These enhancements reduce the encoding quantum bit error rate from 0.29% and 0.58% to 0.18% and 0.37%, which is particularly crucial for high-frequency, high-loss QKD systems. Furthermore, we conducted QKD demonstration experiments to validate the long-term stability of the hybrid integrated module operating at higher clock rates.[37] These results confirm that our hybrid integrated module is capable of supporting an advanced QKD system.

4 Conclusion and Discussion

In this work, we propose a hybrid optoelectronic integrating scheme based on the COB approach for quantum communication applications. Taking into account the functional and performance requirements of quantum bit encoding modules, we have conducted comprehensive optimization in circuit interconnection, structural design, and thermal management, thereby implementing a complete QKD encoding and transmission functionality within a compact, centimeter-scale module. The thermal stability of the module under operational conditions has been verified through both simulations and experiments. Experimental results demonstrate that the module maintains the photonic chip temperature within a specified range even during extended continuous operation, showing close agreement with simulation predictions. Furthermore, the hybrid packaging approach minimizes parasitic effects inherent in PCB interconnects, thereby better preserving signal integrity and enhancing the performance of high-speed QKD systems. This work provides valuable insights and a practical methodology for addressing the engineering challenges in practical QKD system implementation.

Our proposed solution represents a cost-effective approach, building upon relatively mature QKD technologies. Future monolithically integrated optoelectronic QKD systems mayultimately offer superior performance. For instance, the SG25H5 EPIC process developed by the Leibniz Institute for High Performance Microelectronics (IHP) demonstrates the co-integration of BiCMOS technology with silicon photonic devices. However, developing reliable monolithic integration processes remains challenging due to differences in dimensions, fabrication steps, and technical requirements between electronic and photonic components. Despite these challenges, the significant potential of monolithic integration continues to motivate research efforts in this direction. In the interim, hybrid optoelectronic packaging—such as photonic wire bonding between optical chips and 3D integration of electronics and photonics—offers a practical pathway toward miniaturized systems that balance cost and integration level.[38–40] Looking forward, the integration of laser chips with encoding photonic chips via photonic wire bonding, combined with flip-chip bonding of driver electronics, could further enhance the integration level of QKD transmitters.

From the perspective of QKD system design itself, there is also considerable work that can be done to enhance the performance of hybrid optoelectronic integrated systems. On the one hand, optimizing the half-wave voltage of electro-optic modulators in QKD systems to reduce driver circuit requirements represents a crucial aspect for advancing hybrid optoelectronic integration. Current QKD transmitter chips typically exhibit relatively high half-wave voltages in their electro-optic modulators, necessitating driver-amplifier configurations to meet quantum state preparation requirements. This approach not only increases the complexity of driver circuit design but also contributes significantly to overall system power consumption due to the high-voltage demands. Reducing the voltage requirements of QKD encoding chips to align with standard CMOS voltage levels is therefore essential for further promoting the hybrid optoelectronic integration of QKD systems.

On the other hand, improving the security of integrated QKD systems is equally critical to this study. As shown in Fig. 11, the driving signals for the modulators exhibit inherent noise, fluctuations, and jitter, which are unavoidable in practical electronic systems. These non-ideal factors lead to imperfections in quantum state preparation, adversely affecting system performance while

also introducing side-channel risks. To circumvent these side-channel security issues, future development of integrated QKD systems could consider adapting side-channel-free protocol designs[41–43] or fully passive QKD architectures.[44–47] Advancing research in these directions is pivotal for the practical deployment of secure and miniaturized QKD transmitters.

Disclosures

The authors declare no conflict of interest.

Code and Data Availability

All the data and methods needed to evaluate the conclusions of this work are presented in the main text. Additional data are available from the corresponding author upon reasonable request.

Acknowledgments

The authors gratefully acknowledged the University of Science and Technology of China and the SJTU Pinghu Institute of Intelligent Optoelectronics for technical support. This work was supported by the Natural Science Basis Research Plan in Shaanxi Province of China (Grant No. 2025JC-YBQN-043), the National Natural Science Foundation of China (Grant Nos. 62274182 and 62450056), and the Youth Fund Project of Rocket Force University of Engineering (Grant No. 2024QN-B042).

References

1. N. Gisin et al., "Quantum cryptography," *Rev. Mod. Phys.* **74**, 145–195 (2002).
2. F. Xu et al., "Secure quantum key distribution with realistic devices," *Rev. Mod. Phys.* **92**(2), 025002 (2020).
3. X. Ji et al., "Quantum-secured DSP-lite data transmission architecture for AI-driven data centers," *Adv. Photonics* **7**(6), 066006 (2025).
4. Y. Li et al., "Microsatellite-based real-time quantum key distribution," *Nature* **640**(8057), 47–54 (2025).
5. W. Li et al., "High-rate quantum key distribution exceeding 110 Mb s^{-1}," *Nat. Photonics* **17**(5), 416–421 (2023).
6. Y. A. Chen et al., "An integrated space-to-ground quantum communication network over 4,600 kilometres," *Nature* **589**(7841), 214–219 (2021).
7. M. Cherchi et al., "Supporting quantum technologies with an ultralow-loss silicon photonics platform," *Adv. Photonics Nexus* **2**(11), 24002 (2023).
8. "The rise of integrated quantum photonics," *Nat. Photonics* **14**, 265 (2020).
9. W. Luo et al., "Recent progress in quantum photonic chips for quantum communication and internet," *Light: Sci. Appl.* **12**, 175 (2023).
10. Q. Liu et al., "Advances in chip-based quantum key distribution," *Entropy* **24**(10), 1334 (2022).
11. C. Ma et al., "Silicon photonic transmitter for polarization-encoded quantum key distribution," *Optica* **3**(11), 1274 (2016).
12. P. Sibson et al., "Integrated silicon photonics for high-speed quantum key distribution," *Optica* **4**(2), 172–177 (2017).
13. P. Sibson et al., "Chip-based quantum key distribution," *Nat. Commun.* **8**, 13984 (2017).
14. T. K. Paraïso et al., "A modulator-free quantum key distribution transmitter chip," *NPJ Quantum Inform.* **5**(1), 42 (2019).
15. H. Semenenko et al., "Chip-based measurement-device-independent quantum key distribution," *Optica* **7**(3), 238–242 (2020).
16. J. A. Dolphin et al., "A hybrid integrated quantum key distribution transceiver chip," *NPJ Quantum Inform.* **9**(1), 84 (2023).
17. X. Chen et al., "Quantum entanglement on photonic chips: a review," *Adv. Photonics* **3**(6), 064002 (2021).
18. K. Wei et al., "Resource-efficient quantum key distribution with integrated silicon photonics," *Photonics Res.* **11**(8), 1364–1372 (2023).
19. H. Du et al., "Twin-field quantum key distribution with optical injection locking and phase encoding on-chip," *Optica* **11**(10), 1385–1390 (2024).
20. Y. Du et al., "Chip-integrated quantum signature network over 200 km," *Light: Sci. Appl.* **14**, 108 (2025).
21. F. Beutel et al., "Detector-integrated on-chip QKD receiver for GHz clock rates," *NPJ Quantum Inform.* **7**, 40 (2021).
22. W. Pernice et al., "Fully integrated four-channel wavelength-division multiplexed QKD receiver," *Optica* **9**(10), 1121–1130 (2022).
23. Y. Du et al., "Silicon-based decoder for polarization-encoding quantum key distribution," *Chip* **2**(1), 100039 (2023).
24. G. Guarda et al., "Quantum key distribution with a borosilicate-glass-matrix integrated photonic receiver," *Phys. Rev. A* **110**(4), 042605 (2024).
25. A. A. E. Hajomer et al., "Continuous-variable quantum key distribution at 10 GBaud using an integrated photonic-electronic receiver," *Optica* **11**(9), 1197–1204 (2024).
26. Y. Bian et al., "Continuous-variable quantum key distribution over 28.6 km fiber with an integrated silicon photonic receiver chip," *Appl. Phys. Lett.* **124**, 174001 (2024).
27. Z. Lin et al., "Integrated lithium niobate photonics for high-speed quantum key distribution," *Optica Quantum* **3**(2), 195 (2025).
28. H. Heo et al., "On-chip quantum key distribution over field-deployed fiber using lithium niobate photonic circuit," *APL Photonics* **10**(3), 031301 (2025).
29. R. Sax et al., "High-speed integrated QKD system," *Photonics Res.* **11**(6), 1007 (2023).
30. H. Yue et al., "Silicon modulator exceeding 110 GHz using tunable time-frequency equalization," *Optica* **12**(2), 203–215 (2025).
31. X. Li et al., "Single-drive high-speed lumped depletion-type modulators toward 10 fJ/bit energy consumption," *Photonics Res.* **5**(2), 134–142 (2017).
32. X. Xiao et al., "High-speed, low-loss silicon Mach–Zehnder modulators with doping optimization," *Opt. Express* **21**(4), 4116–4125 (2013).
33. Z.-Y. Chen et al., "A 1.25-GHz multi-amplitude modulator driver in 0.18 μm SiGe BiCOMOS technology for high speed quantum key distribution," *Rev. Sci. Instrum.* **94**, 104703 (2023).
34. D. Bunandar et al., "Metropolitan quantum key distribution with silicon photonics," *Phys. Rev. X* **8**(2), 021009 (2018).
35. K. Wei et al., "High-speed measurement-device-independent quantum key distribution with integrated silicon photonics," *Phys. Rev. X* **10**(3), 031030 (2020).
36. C.-X. Zhu et al., "Experimental quantum key distribution with integrated silicon photonics and electronics," *Phys. Rev. Appl.* **17**(6), 64034 (2022).
37. Z.-Y. Chen et al., "Integrated photonics and electronics for high-speed quantum key distribution," *Laser Photonics Rev.*, e01080 (2025).
38. W. Tian et al., "Progress in research on co-packaged optics," *Micromachines* **15**(10), 1211 (2024).
39. M. Tan et al., "Co-packaged optics (CPO): status, challenges, and solutions," *Front. Optoelectron.* **16**, 1 (2023).
40. D. Liang and J. E. Bowers, "Recent progress in heterogeneous III-V-on-silicon photonic integration," *Light: Adv. Manuf.* **2**(1), 59–83 (2021).
41. X. B. Wang, X. L. Hu, and Z. W. Yu, "Practical long-distance side-channel-free quantum key distribution," *Phys. Rev. Appl.* **12**, 054034 (2019).
42. C. Zhang et al., "Experimental side-channel-secure quantum key distribution," *Phys. Rev. Lett.* **128**, 190503 (2022).
43. C. Jiang et al., "Side-channel security of practical quantum key distribution," *Phys. Rev. Res.* **6**, 013266 (2024).
44. W. Wang et al., "Fully passive quantum key distribution," *Phys. Rev. Lett.* **130**, 220801 (2023).

45. F.-Y. Lu et al., "Experimental demonstration of fully passive quantum key distribution," *Phys. Rev. Lett.* **131**, 110802 (2023).
46. C. Hu et al., "Proof-of-principle demonstration of fully passive quantum key distribution," *Phys. Rev. Lett.* **131**, 110801 (2023).
47. A. Gnanapandithan, L. Qian, and H.-K. Lo, "Hidden multidimensional modulation side channels in quantum protocols," *Phys. Rev. Lett.* **134**, 130802 (2025).

Zhao-Yuan Chen is a lecturer at the Rocket Force University of Engineering. He received his BS degree in optics from the University of Science and Technology of China in 2017 and his MS degree and PhD from the Rocket Force University of Engineering in 2019 and 2024, respectively. His current research interests include quantum communication and integrated optoelectronic systems.

Biographies of the other authors are not available.