Microelectronics Journal 173 (2026) 107165

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

A high-gain transimpedance amplifier with pulse widening suppression for pulsed ToF Lidar receiver applications

Hao Zheng [a], Yanming He [a], Xiayu Wang [b], Dong Li [b], Yanfei Liu [a], Zhaoyuan Chen [a], Rui Ma [b,*]

[a] Rocket Force University of Engineering, Xi'an, 710025, China
[b] Key Laboratory of Analog Integrated Circuits and Systems (Ministry of Education), School of Integrated Circuits, Xidian University, Xi'an, 710071, China

ARTICLE INFO

Index Terms:
Pulsed LiDAR
Pulse widening suppression
Transimpedance amplifier
Time-of-flight

ABSTRACT

A high-gain transimpedance amplifier (TIA) is proposed for pulsed time-of-flight (ToF) LiDAR receiver applications, consisting primarily of a shunt-feedback transimpedance preamplifier (SF-preTIA), a post voltage amplifier, and an output buffer. The SF-preTIA is responsible for converting the input photocurrent into a corresponding voltage signal. To suppress the widening of output pulse voltage when dealing with high input currents, a novel pulse widening suppression (PWS) scheme is proposed, which adopts a diode-connected MOS pair in parallel with the feedback resistor. Furthermore, the parasitic capacitance of the MOS pair is utilized to compensate for the frequency response of the TIA, thereby alleviating potential stability issues of the SF-TIA. Specifically, the post voltage amplifier is designed to improve the output voltage swing, while the output buffer is dedicated to enhancing the driving capability for external loads. Implemented in a 0.18 μm standard CMOS process, post-layout simulation results demonstrate that the proposed TIA achieves a transimpedance gain of ~106 dBΩ, a −3 dB bandwidth of ~234 MHz, and an average input-referred noise (IRN) current spectral density of 3.5 pA/sqrt(Hz). When a high input current with an amplitude of 10 mA and a full-width at half-maximum (FWHM) of 3.6 ns is applied, the output voltage pulse widening of the TIA with the PWS scheme is only 10% of that without the scheme.

1. Introduction

Recently, the light detection and ranging (LiDAR) sensors adopting pulsed time of flight (ToF) method become indispensable for the applications demanding precise, long-range and real-time distance measurements, such as autonomous driving, intelligent robotics, unmanned aerial vehicles (UAVs) and unsupervised home monitoring [1–4]. In a pulsed ToF Lidar system, the receiver primarily consists of a photoelectric detector (PD) and an analog front-end (AFE) circuit. The PD are used to convert pulsed echo signals into electrical current, and avalanche photodiodes (APDs) operating in linear mode are widely favored as PD candidates in LiDAR receivers, attributed to their high sensitivity, short dead time and capability of capturing intensity information [5,6]. The core function of AFE circuit is to identify the timing point via a timing discriminator when the pulse echo stamps the PD. However, since the PD output is a current signal, a transimpedance amplifier (TIA) is typically inserted between the PD and timing discriminator to convert and amplify the photogenerated current from the PD into a voltage signal with sufficiently large amplitude.

In linear-mode pulsed LiDAR receivers, the timing comparator often suffers from the so-called "walk error" caused by the variations in echo signal intensity, which directly degrades the accuracy of distance measurement [7]. Walk error compensation is a well-established approach to enhance timing discrimination accuracy, among which the pulse width compensation scheme has proven effective and is documented in several literatures [8–10]. Nevertheless, the validity of pulse width-based walk error compensation relies on a critical premise: the output voltages of echo signals with varying intensities must not exhibit significant widening at the TIA output terminal. Otherwise, this compensation strategy will be invalid. In practice, the conventional shunt-feedback TIA (SF-TIA) tends to experience output voltage pulse widening due to saturation distortion when subjected to high-input currents [11], which will be elaborated in Section 2.

Thus, the pulse widening phenomenon imposes inherent limitations on the performance of pulse width-based walk error compensation. To address this issue, this work proposes a multi-stage transimpedance amplifier with pulse widening suppression (PWS-TIA), which comprises a transimpedance preamplifier (preTIA), a post voltage amplifier (PVA)

* Corresponding author.
E-mail address: rma@xidian.edu.cn (R. Ma).

https://doi.org/10.1016/j.mejo.2026.107165
Received 11 January 2026; Received in revised form 17 February 2026; Accepted 7 March 2026
Available online 9 March 2026
1879-2391/© 2026 Published by Elsevier Ltd.

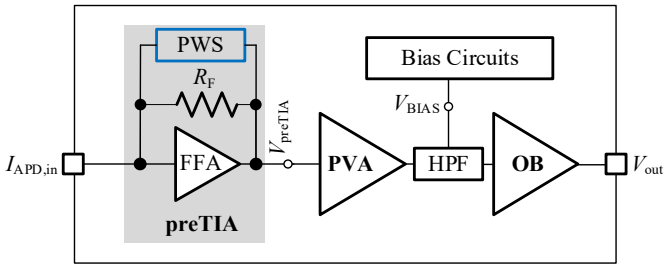


Fig. 1. Simplified block diagram of the proposed transimpedance amplifier.

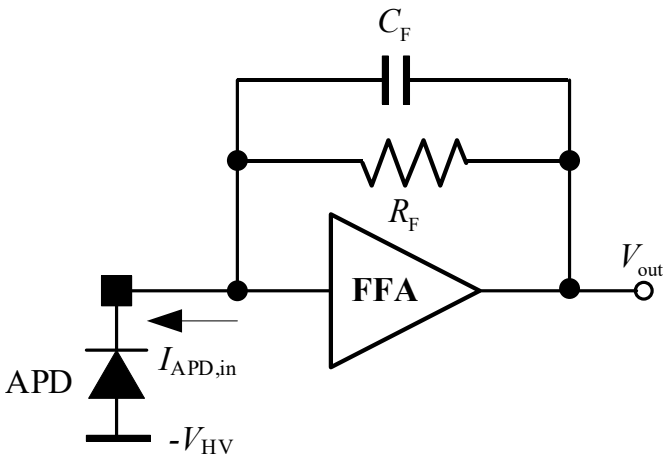


Fig. 2. Typical SF-TIA with frequency compensation.

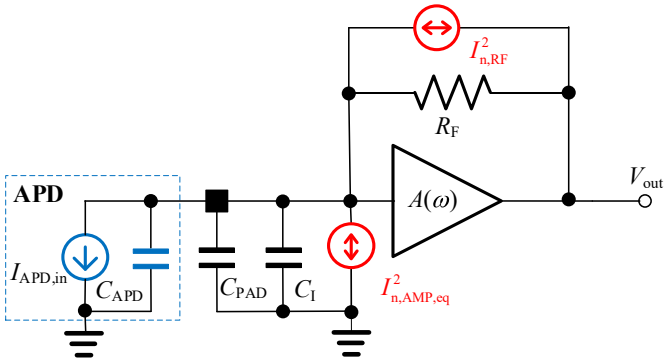


Fig. 3. Simplified noise model of the SF-TIA topology.

with a high-pass filter (HPF), and an output buffer (OB), as illustrated in Fig. 1. The preTIA serves as a current-to-voltage converter, while the subsequent PVA further amplifies the voltage swing from the preTIA output. The final OB stage is designed to enhance the driving capability for external loads. The remainder of this paper is structured as follows: Section 2 discusses the design issues of the AFE circuit; Section 3 presents and analyzes the key circuit components of the proposed AFE; Section 4 provides the simulation results; and Section 5 summarizes the conclusions.

2. Design issues of TIA

In AFE circuit of pulsed Lidar receiver, SF-TIA topology boasts more advantages over the regulated cascode TIA (RGC-TIA), such as wider bandwidth, better noise feature, and higher output swing in low voltage design [6]. Fig. 2 shows a typical SF-TIA, which mainly consists of a feedforward amplifier (FFA), a feedback resistor (R_F) and a feedback capacitor (C_F). The feedback capacitor is commonly used to obtain enough phase margin by means of frequency compensation.

To effectively detect input current signals at the microampere level, the noise of the front-end circuit should be minimized as much as possible to improve the signal-to-noise ratio, aiming to reduce the false alarm probability. Fig. 3 illustrates the noise contributors in SF-TIA, which mainly include the noise from the feedback resistor (R_F) and the noise from the FFA. The power spectral density (PSD) of the input-referred noise (IRN) current spectral density can be expressed by [12].

$$I^2_{n,in,TIA}(f) = \frac{4kT}{R_F} + 4kT\Gamma\left(\frac{1}{g_m R_F^2} + \frac{(2\pi C_T)^2 f^2}{g_m}\right) \quad (1)$$

where k denotes Boltzmann's constant, T is the absolute temperature, Γ represents Ogawa's excess noise factor, g_m is the transconductance of the input transistor, and C_T denotes the total parasitic capacitance at the input terminal of the TIA. C_T is approximately equal to $C_{APD} + C_{PAD} + C_I$, where C_{APD} is the parasitic capacitance of the APD, C_{PAD} is the parasitic capacitance of the bonding pad, C_I is the parasitic capacitance at the input terminal of the feedforward amplifier. Eq. (1) indicates that a higher transimpedance gain (R_F), a larger transconductance (g_m), and a minimizing the total input capacitance (C_T) can synergistically reduce the IRN current. However, an excessively high resistance value will cause premature saturation of the TIA output voltage, thereby inducing the output voltage pulse widening phenomenon. For short-distance detection and/or strong-reflected objects, the receiver AFE circuit is required to process high-current echo signals. Consequently, the pulse widening phenomenon will be further exacerbated due to the high-resistance feedback resistor.

To address the aforementioned issues, conventional approaches adopt programmable schemes that adjust the transimpedance gain to accommodate echo current signals of varying intensities [13–16]. For instance, in the case of high-input-current signals, the transimpedance gain can be reduced by gating switches controlled by gain control bits, which ensures that the output waveform avoids saturation and prevents pulse widening. Additionally, the automatic gain control (AGC) method is employed to dynamically adjust the transimpedance gain [4,17]. However, these methods entail relatively complex practical circuit implementations and often fail to deliver the expected performance. Recently, the SF-TIA architectures integrated with reverse current cancellation (RCC) circuit have been proposed to accelerate the output voltage recovery time under large input current [11]. While the

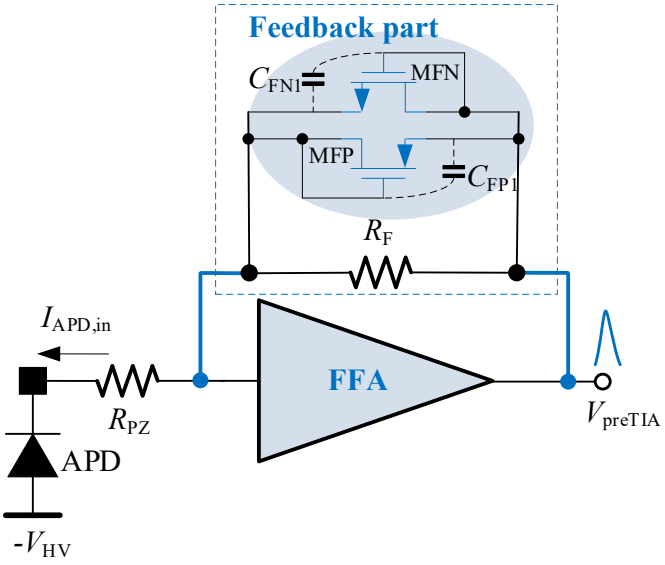


Fig. 4. Schematics of proposed transimpedance preamplifier with diode-connected MOS pair.

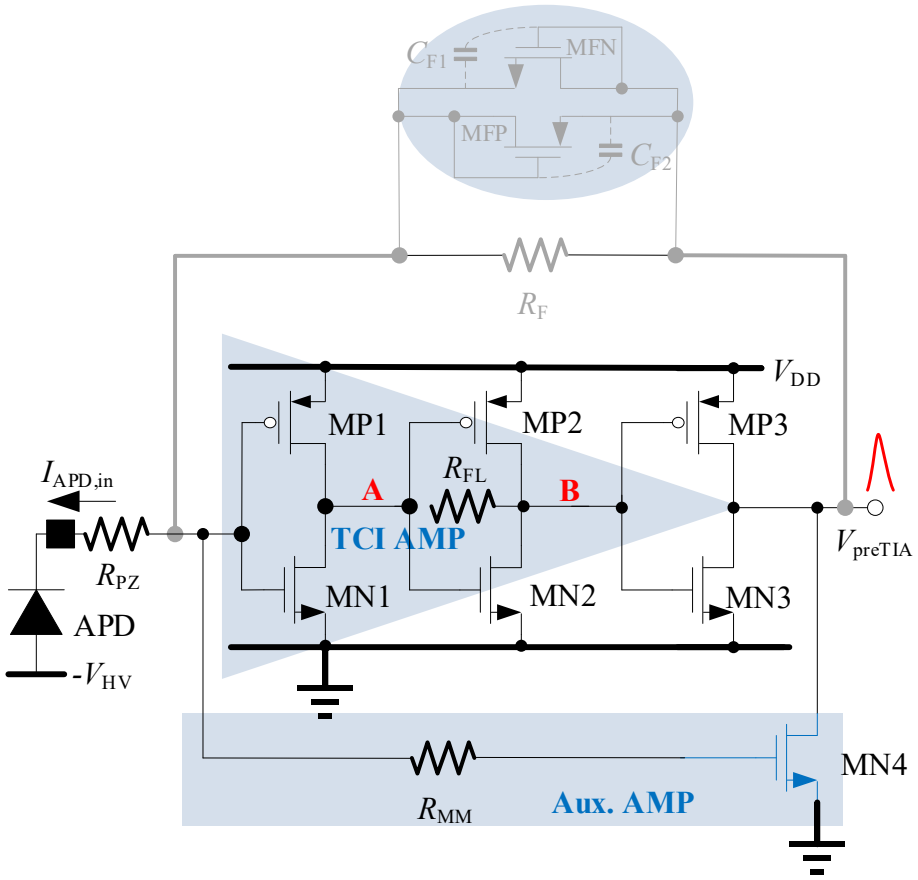


Fig. 5. Schematics of proposed feedforward amplifier.

approach introduced in Ref. [11] serves to steepen the pulse falling edge, the measured results demonstrate that the echo pulse widening effect is still distinctly observable.

3. Circuits implementation

To address the pulse widening issue induced by high-input current conditions in conventional TIAs, this work proposes a TIA with integrated pulse widening suppression capability. Specifically, when subjected to high photocurrent inputs, the proposed PWS-TIA can effectively mitigate the pulse widening phenomenon caused by saturation distortion. As outlined previously, the proposed architecture is primarily composed of a preTIA, a PVA and an OB. This section elaborates on the circuit-level implementation details of the proposed PWS-TIA.

3.1. Transimpedance preamplifier

The preTIA functions as a current-to-voltage converter, with the schematics of the proposed preTIA illustrated in Fig. 4. This circuit architecture primarily consists of a FFA and a feedback part. In contrast to the traditional SF-TIA shown in Fig. 2, a diode-connected MOS pair (MFN and MFP) is paralleled across the feedback resistor (R_F), and both serve as the feedback part. For the low-input-current conditions, the voltage across R_F is lower than the threshold voltages (V_{TH}) of the MOS pair, resulting that the diode-connected MOS pair is in the off state. When a high-input-current is applied, the output voltage rises sharply and exceeds V_{TH} by a significant margin, triggering the turn-on of the diode-connected MOS pair. Under this condition, the current-voltage relationship of the MOS pair closely follows the characteristic equation of a transistor operating in saturation mode. Thus, the total feedback current can be expressed as

$$i_F = \frac{V_{gs}}{R_F} + \frac{1}{2}C_{ox}\left[\mu_n\left(\frac{W}{L}\right)_{MFN}\left(V_{gs} - V_{TH,MFN}\right)^2 + \mu_p\left(\frac{W}{L}\right)_{MFP}\left(-V_{gs} + V_{TH,MFP}\right)^2\right] \tag{2}$$

where V_{gs} is the gate-source voltage of the MFN, and equal to the pulse amplitude (V_{preTIA}) of the preTIA output voltage, μ_n and μ_p are the mobilities of NMOS and PMOS, respectively, $V_{TH,MFN}$ and $V_{TH,MFP}$ are the threshold voltages of the MFN and MFP, respectively, $(W/L)_{MFN}$ and $(W/L)_{MFP}$ denote the width to length ratios of the MFN and MFP, respectively.

In fact, when a pulse current with moderate magnitude is injected into the input of the preTIA, and the output voltage amplitude of the preTIA is approximately equal to the threshold voltage of the MOS pair, the diode-connected MOS pair operates in the sub-threshold region. Under this condition, the feedback current can be approximately expressed by

$$i_F = \frac{V_{gs}}{R_F} + I_0 e^{\frac{V_{gs}}{\zeta V_T}} \tag{3}$$

where $\zeta > 1$ is a nonideality factor, and $V_T = kT/q$.

For simplicity, only the case where the transistor operates in the saturation region under high-input current is considered in this design. Consequently, the equivalent low-frequency transimpedance gain can be approximated as:

$$Z_{T,eq} = R_F \Big/\!\Big/ \frac{1}{g_{m,MFN}} \Big/\!\Big/ \frac{1}{g_{m,MFP}} \tag{4}$$

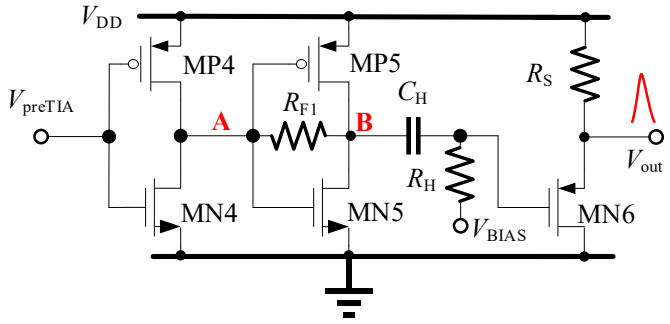


Fig. 6. Schematics of proposed PVA and OB.

where $g_{m,MFN}$ and $g_{m,MFN}$ are the transconductances of the MFN and MFP, respectively.

Considering the potential stability issues associated with the SF-TIA, a capacitor is typically connected in parallel with the feedback resistor, as depicted in Fig. 2. In this work, the gate-source parasitic capacitances of the diode-connected MOS pair are exploited to compensate the frequency response of the proposed preTIA. As a result, the feedback capacitor (C_F) shown in Fig. 2 can be omitted. The total gate-source parasitic capacitance ($C_{F,par}$) of the diode-connected MOS pair in Fig. 4 is approximated as

$$C_{F,par} = C_{FN1} + C_{FP1} \approx \frac{2}{3} C_{ox}(W_{MFN}L_{MFN} + W_{MFP}L_{MFP}) \tag{5}$$

where C_{ox} is the gate oxide capacitance per unit area. In this design, the total parasitic capacitances of ~30 fF are specifically introduced.

To break the trade-off between transimpedance gain and bandwidth in the TIA [18], the bandwidth of the FFA typically needs to be maximized. The proposed feedforward amplifier adopts the circuit structure illustrated in Fig. 5, which mainly consists of a main FFA with three cascaded inverter-type amplifiers (TCI AMP) and an auxiliary amplifier (Aux. AMP) featuring a common-source structure. Within the TCI AMP, the local feedback resistor R_{FL} ensures the proper DC biasing for nodes A and B. The MN4 functions as the feedforward path, which enhances the stability and boost the bandwidth of the preTIA. Meanwhile, the R_{MM} is employed to suppress the overshoot caused by the input bonding wire [13,19]. The resistor R_{PZ}, inserted between the bonding pad and the preTIA input, is employed to further enhance the phase margin of the SF-preTIA by introducing a phantom zero [20].

3.2. Post voltage amplifier and output buffer

Owing to the constrained transimpedance gain of the preTIA, its output signal typically exhibits a low amplitude. To address this issue, a PVA is cascaded to the preTIA output terminal as the subsequent stage, serving to boost the signal swing. Additionally, the OB is required to improve the driving capability for the external load when the TIA circuit is measured. Fig. 6 shows the schematics of the proposed PVA and OB.

In Fig. 6, the cascaded inverter-type amplifiers act as PVA, with R_{F1} serving to set the common-mode voltage of these inverter-type amplifiers. The OB consists of a high-pass filter (HPF) and a common-drain amplifier, which are employed to filter the low frequency noise and enhance the driving capability for the external load, respectively. Meanwhile, the DC level of the MN3 gate is established by the bias circuits (V_{BIAS}). The dc gain of the PVA can be expressed as

$$A_{u,PVA} = \frac{g_{M4}g_{M5}(R_{F1}//r_{ds4})\left(1-\frac{1}{g_{M5}R_{F1}}\right)}{g_{M5}(R_{F1}//r_{ds4})\left(1-\frac{1}{g_{M5}R_{F1}}\right)\frac{1}{R_{F1}}+\frac{1}{R_{F1}//r_{ds5}}} \tag{6}$$

where $g_{M4} = g_{m,MN4}+g_{m,MP4}$, with $g_{m,MN4}$ and $g_{m,MP4}$ denoting the transconductances of the MN4 and MP4, respectively. $g_{M5}=g_{m,MN5}+g_{m,MP5}$, where $g_{m,MN5}$ and $g_{m,MP5}$ represent the transconductances of the MN5 and MP5, respectively. r_{ds4} is the small-signal output resistance of the inverter-type amplifier formed by MN4 and MP4, while r_{ds5} is the small-signal output resistance of the inverter-type amplifier consisting of MN5 and MP5. In this design, since $g_{M5}R_{F1} \gg 1$ and $g_{M5}(R_{F1}//r_{ds2}) \gg 1$, Eq. (6) can be approximated as

$$A_{u,PVA} \approx g_{M4}R_{F1} \tag{7}$$

Accordingly, the total middle-frequency gain of the PVA and OB can be expressed as

$$A_{u,PVA+OB} \approx g_{M4}R_{F1}\frac{g_{M6}R_S}{1+g_{M6}R_S}\frac{sC_HR_H}{1+sC_HR_H} \tag{8}$$

Table 1
Main device sizes and resistor values of proposed TIA circuits.

Devices	W/L (μm/μm)	Devices	W/L (μm/μm)	Resistors	Value(Ω)
MP1	40/0.18	MN1	20/0.18	R_F	10k
MP2	5/0.18	MN2	2.5/0.18	R_{FL}	1.6k
MP3	20/0.18	MN3	10/0.18	R_{MM}	1.5k
MFN	10/0.3	MFP	10/0.3	R_{PZ}	115
MFF	10/0.5	MN6	20/0.18	R_{F1}	2.2k
MP4	40/0.18	MN4	20/0.18	R_H	150k
MP5	36/0.18	MN5	10/0.18		

3.3. Noise analysis and optimization

In the AFE circuit, the noise performance of the TIA fundamentally determines the sensitivity of the LiDAR receiver, rendering the noise analysis and optimization of the TIA critically significant. For the proposed PWS-TIA, the diode-connected MOS pair remains in the off-state under low-input-current conditions, thereby exerting a negligible influence on the TIA's noise performance. Consequently, the noise component of the MOS pair can be omitted during noise analysis.

The noise analysis presented herein is based on the van der Ziel MOSFET noise model [17]. Given that the proposed TIA typically operates in the high-frequency range, thermal noise is considered the dominant noise source, while the flicker noise of MOSFETs is generally neglected. In multistage TIA configurations, the preTIA constitutes the primary noise contributor, as its noise is further amplified by subsequent stages. The total IRN current spectral density is given by

$$I^2_{n,in,tot} \approx \frac{4kT}{R_F} + 4kT\left[\Gamma\left(\frac{1}{g_{m,MN1}+g_{m,MP1}}+\frac{1}{g_{m,MN4}}\right)+\frac{R_C^2}{R_F}+R_C+R_{MM}\right](4\pi^2C_T^2f^2) \tag{9}$$

For short-channel MOS device, the channel thermal noise factor (Γ) is typically equal to 4/3 [21]. Similarly, the adoption of a high-value feedback resistor can directly reduce the lower limit of the IRN as given in Eq. (9). In Eq. (9), the channel noises of the MN1 and MP2 are directly coupled to the input terminal of the TIA. Consequently, increasing the transconductances of MN1, MP2 and MN4 serves to decrease the IRN current. Meanwhile, on the premise of guaranteeing system stability, the use of low-value resistors (R_C and R_{MM}) and the reduction of total input capacitance (C_T) are beneficial for enhancing the overall noise performance of the transimpedance amplifier.

4. Post-layout simulation results

The proposed TIA was designed and simulated using the Spectre simulator on the Cadence Virtuoso platform, with its performance verified in a 0.18 μm standard CMOS process under a 1.8 V supply voltage. The main transistor aspect ratios and resistors of the preTIA circuit are shown in Table 1. The layout of the proposed TIA core is

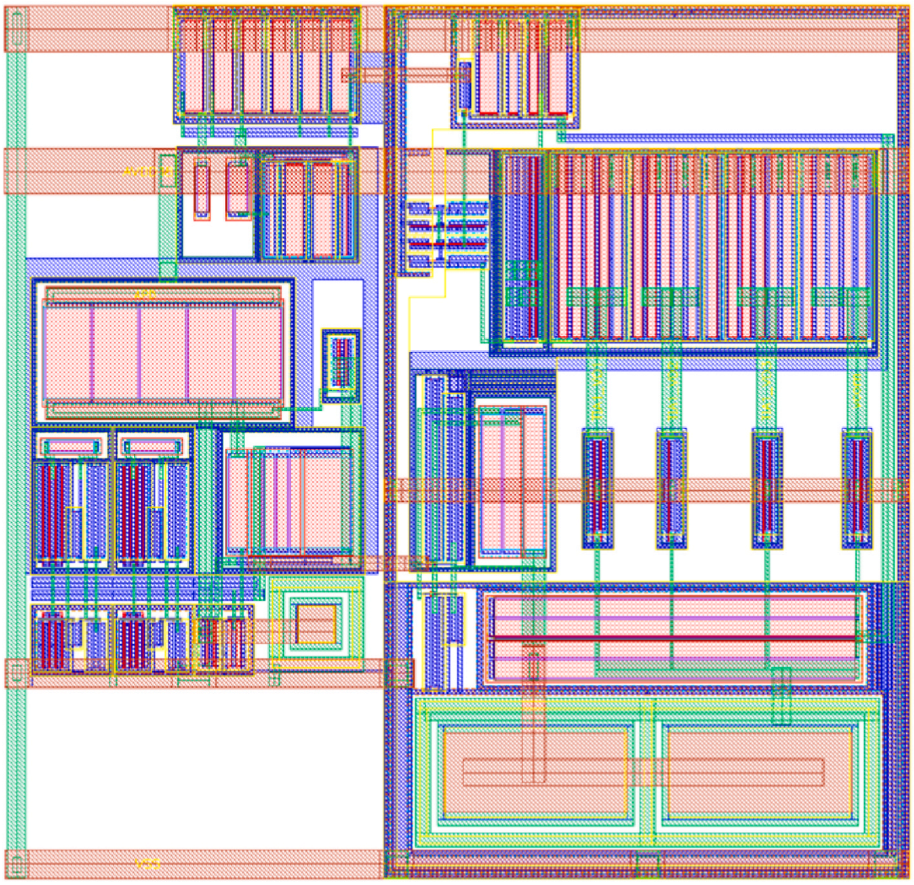


Fig. 7. Layout of proposed TIA.

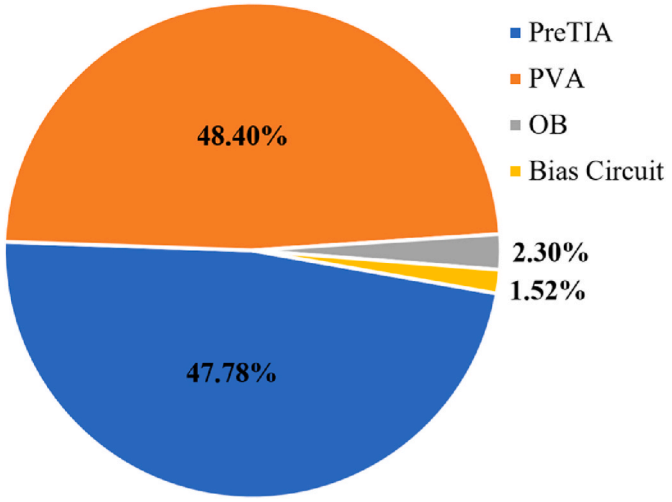


Fig. 8. Power consumption breakdown of the proposed TIA.

shown in Fig. 7, with an active area of 100 μm × 97 μm. The power consumption of the circuit core is about 11.7 mW for 1.8 V power supply, Fig. 8 shows the power consumption breakdown of the proposed TIA, where most of the power is consumed by the preTIA and PVA.

Transient simulations incorporating device noise were conducted to investigate the transient characteristics of the proposed TIA. The input currents with rise time of ~2.0 ns are typically applied, Fig. 9 depicts the simulated output waveforms of the proposed TIA under low-input-current conditions. Fig. 9 (a) shows the output voltage waveforms for the input currents ranging from 0.2 μA to 1 μA. In this case, the output voltage amplitudes are below 212 mV, and the MOS pair operates in the cut-off state. As the input current increases to approximately 2 μA, the output voltage amplitude approaches the threshold voltage of the MOS pair, and the MOS pair enters the subthreshold region. When the input current exceeds approximately 3 μA, the MOS pair operates in the saturation region, with the corresponding output waveforms shown in Fig. 9(b). It can be observed from Fig. 9 that the proposed TIA achieves effective amplification for various pulse input currents. In Fig. 9 (b), when an input current with amplitude of 1.0 μA is applied to the proposed TIA, the output voltage amplitude reaches approximately 212 mV, leading to a calculated transimpedance gain of around 106.5 dBΩ. Meanwhile, the simulated root-mean-square (RMS) value at the output noise of the proposed TIA is approximately 22 mV.

To evaluate the pulse widening suppression performance of the proposed TIA under high-input-current conditions, transient simulations were performed on both the conventional SF-TIA and the proposed TIA. Fig. 10 presents the transient simulation results of the TIA output terminal for input current pulses with a full-width at half-maximum (FWHM) of ~3.6 ns. For the conventional SF-TIA illustrated in Fig. 2, the output voltage pulse exhibits a widening effect when a high current is applied, with the simulated waveforms shown in Fig. 10(a). As observed in Fig. 10(a), the widening of the output voltage pulse becomes distinctly pronounced when the input current exceeds 100 μA. At input currents of 1.0 mA and 10 mA, the output voltage pulse widths are 20 ns and 54 ns, respectively. In contrast, the pulse widening phenomenon is significantly suppressed in the SF-TIA integrated with a diode-connected MOS pair under high-input-current conditions, as shown in Fig. 10(b). For input currents of 1 mA and 10 mA, the output voltage pulse widths are reduced to 6.6 ns and 8.7 ns, respectively. Consequently, when an input current of 10 mA is applied, the output voltage pulse width expansion of the TIA with PWS is only ~10% of that of the TIA without

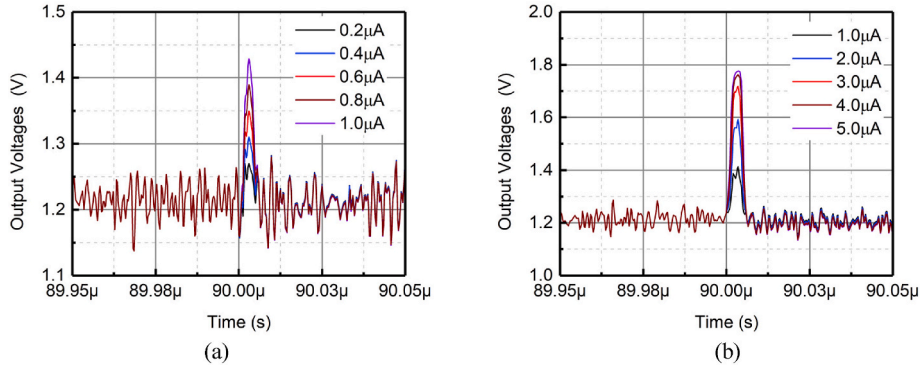


Fig. 9. Transient simulated results of proposed TIA at different input currents (a) when input currents ranging from 0.2 μA to 1.0 μA are applied and (b). when input currents ranging from 1.0 μA to 5.0 μA are applied.

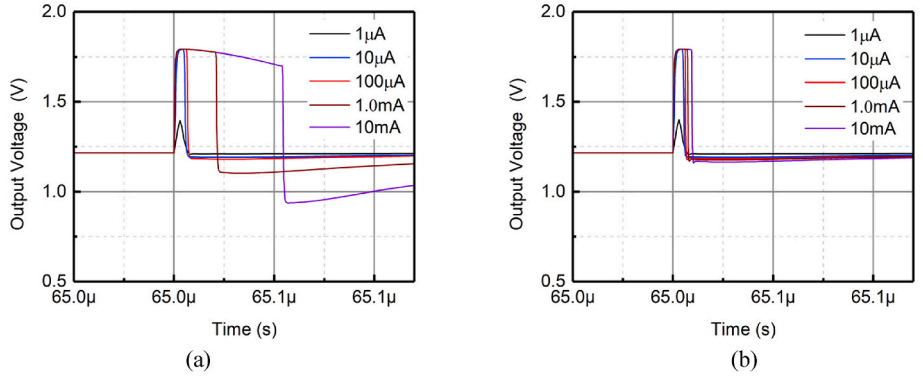


Fig. 10. Transient simulation results of (a) the traditional SF-TIA and (b) the proposed TIA with diode-connected MOS pair.

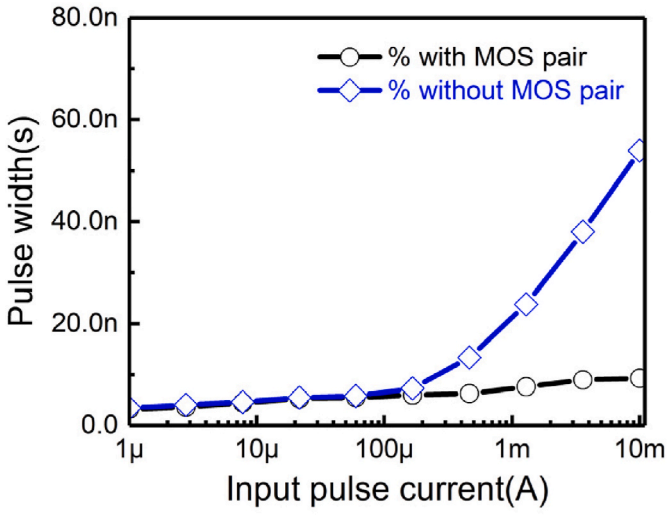


Fig. 11. Simulated results of the pulse width of the proposed TIA and traditional TIA when different input pulse currents with FWHM of 3.6 ns are fed.

the pulse widening suppression.

Fig. 11 shows the output voltage pulse widths for input pulse currents of varying amplitudes, where the input pulses have an FWHM of ~3.6 ns. The blue fitted line in Fig. 11 denotes the output voltage pulse width of the conventional SF-TIA, while the black line represents that of the proposed TIA. Evidently, pulse widening is effectively suppressed in the proposed TIA architecture.

Fig. 12 shows the simulated eye-diagrams of the proposed TIA at the data rates of (a) 1 Gb/s and (b) 500 Mb/s for input current amplitudes of 2 μA. The simulated results demonstrate that the output exhibits clean and wide eye openings.

To simulate the frequency response of the proposed TIA, parasitic elements arising from the external APD and bonding pads were incorporated at the TIA input terminal. In this simulation, a total parasitic capacitance of 1.5 pF was introduced at the input terminal of the proposed TIA. Fig. 13 presents the simulated transimpedance gain characteristics of the proposed TIA, which achieves a −3 dB bandwidth of ~234 MHz and an overall transimpedance gain ($Z_{T,total}$) of ~106 dBΩ. This gain is defined as the product of the transimpedance gain of the pre-TIA, the voltage gain of the PVA, and the voltage gain of the OB. Based on the simulation results, narrow pulse signals with a rise time of ~1.5 ns can be effectively detected. Additionally, the results in Fig. 13 demonstrate that the transimpedance gain frequency response curves exhibit negligible discrepancies across different model corners. Table 2 summarizes the simulated transimpedance gain and bandwidth of the proposed TIA under varying temperatures and process corners. As observed in Table 2, the variation in transimpedance gain is relatively minor and can be neglected. In contrast, the bandwidth undergoes a significant variation, with a minimum value of 172 MHz and a maximum value of 269 MHz. Thus, process corners exert a substantial influence on the bandwidth, primarily due to the large variation in the parasitic capacitance of the diode-connected MOS pair under different process corner conditions. In fact, for a given process corner, the bandwidth variation is approximately 10% over the temperature range of −25 °C to 85 °C, which constitutes an acceptable performance outcome.

The IRN current spectral density of the proposed TIA was simulated, with the results depicted in Fig. 14. The minimum IRN current spectral density is approximately 1.3 pA/sqrt(Hz) over the high-frequency range of 1.0 MHz to 1.0 GHz. Based on the simulated output noise RMS value (22 mV), the calculated average IRN current spectral density is

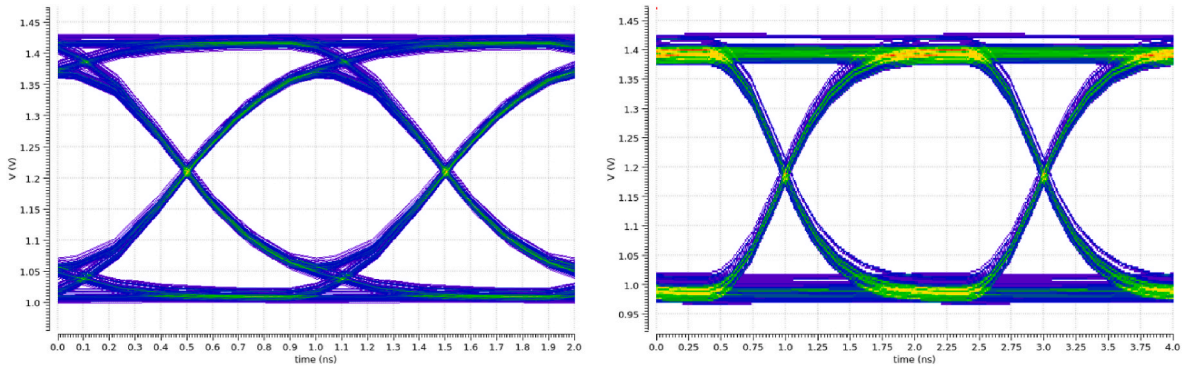


Fig. 12. Simulated eye-diagrams of the proposed TIA at the data rates of (a) 1 Gb/s and (b) 500 Mb/s for input current amplitudes of 2 μA.

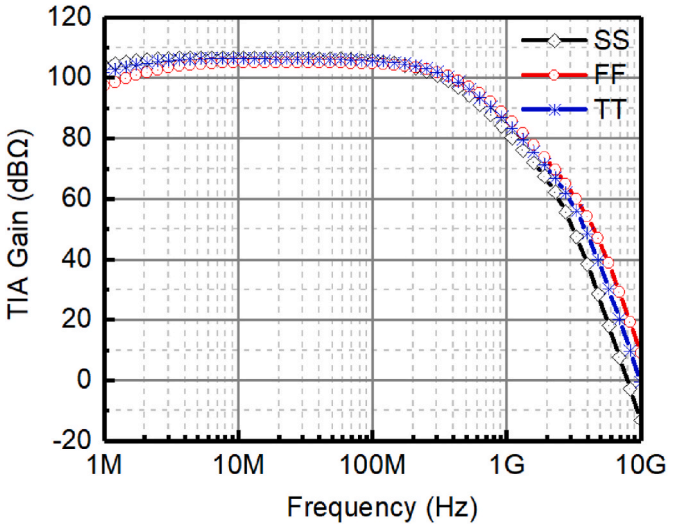


Fig. 13. Simulated transimpedance gain results of proposed TIA at different model corners.

approximately 3.5 pA/sqrt(Hz). The total IRN current RMS was calculated by integrating the simulated noise current spectral density up to 1.0 GHz, yielding a value of ~0.37 μA.

Finally, Table 3 summarizes the key performance metrics of the proposed receiver and compares them with the previously reported CMOS TIAs. Compared with the designs in Refs. [4,17] that employ AGC scheme, the proposed TIA offers superior performance in terms of dynamic range, noise characteristics, and power consumption. Relative to Ref. [11], it exhibits a wider bandwidth, more excellent noise performance, and higher transimpedance gain. In contrast to Refs. [13,14], the proposed TIA integrates the pulse widening suppression (PWS) scheme with a diode-connected MOS pair, eliminating the need for external gain control—a distinct advantage. Overall, the proposed TIA demonstrates comprehensive performance superiority. To make a fair comparison of the performance among different TIAs in pulsed ToF Lidar receiver, we defined the Figure of Merit (FoM) as [2].

$$\mathrm{FoM} = \frac{Z_{\mathrm{T,tot}}\ (\mathrm{dB\Omega}) \cdot BW_{-3\mathrm{dB}}(\mathrm{GHz}) \cdot C_{\mathrm{PD}}(\mathrm{pF})}{\overline{I_{\mathrm{n,in,eq}}}\left(\mathrm{pA}/\sqrt{\mathrm{Hz}}\right)} \tag{10}$$

where $\overline{I_{\mathrm{n,in,eq}}}$ is the average IRN current spectral density. In Tables 3 and it is clearly seen that FoM (10.63) of the proposed TIA exhibits significant advantages over the previous work [17], and is comparable to those reported in Refs. [11,13].

$$\&\overline{I_{\mathrm{n,in,eq}}} = \frac{V_{\mathrm{n,out,RMS}}}{Z_{\mathrm{R,tot}}\sqrt{BW_{\mathrm{n}}}}$$

$$\&\&\mathrm{FoM} = \frac{Z_{\mathrm{T,tot}}\ (\mathrm{dB\Omega}) \cdot BW_{-3\mathrm{dB}}(\mathrm{GHz}) \cdot C_{\mathrm{PD}}(\mathrm{pF})}{\overline{I_{\mathrm{n,in,eq}}}\left(\mathrm{pA}/\sqrt{\mathrm{Hz}}\right)}$$

5. Conclusion

A high-gain TIA is designed and verified in a 0.18 μm CMOS process for pulsed ToF LiDAR applications. The proposed TIA incorporates a

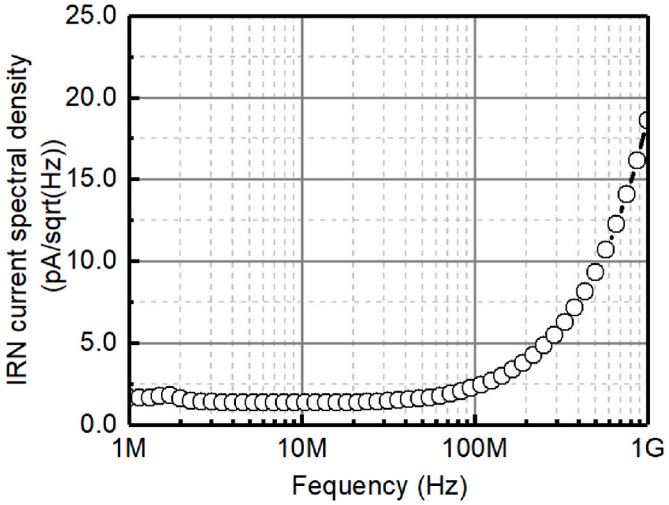


Fig. 14. Simulated IRN current spectral density of proposed TIA.

Table 2
Simulated results of gain and bandwidth of proposed TIA at different temperatures and process corners.

Process Corner	SS			TT			FF		
Temperature (°C)	−25	25	85	−25	25	85	−25	25	85
Transimpedance Gain (dBΩ)	107.7	106.6	105.6	107.4	106.3	105.2	106.2	105.1	104.1
Bandwidth (MHz)	211	191	172	257	234	209	314	290	269
Phase Margin(degree)	81.5	85.5	85.3	83.8	93.1	95.4	92.3	101.5	102.7

Table 3
Performance comparison of recently published receiver.

Parameters	[4]2025	[11]2025	[13]2023	[14]2018	[15]2024	[17]2018	This work[a]
CMOS Technology (nm)	180	180	180	180	180	180	**180**
Supply Voltage (V)	1.8	-	3.3	3.3	1.8	3.3	**1.8**
C_{PD}(pF)	0.49[b]	2.5	1.5	1.5	3.0	1.0	**1.5**
$Z_{T,tot}$(dB Ω)	67.6	102	100	106	100	106	**106**
BW_{-3dB} (MHz)	2140	151	260	153	180	150	**234**
$\overline{I_{n,in,eq}}$ (pA/sqrt(Hz))[&]	-	3.51	3.3	0.89	2.1[d]	4.55	**3.5**
DR(dB)	57.5		79.3	80	52	66	**80**
PWS Scheme	AGC	without	Prog.[c]	Prog.	Prog.	AGC	**MOS pair**
Core area(mm^2)	0.206 × 0.056	0.741	0.11 × 0.11	1.2 × 1.13 (whole chip)	5/8	0.95 × 0.95 (whole chip)	**0.1 × 0.097**
Power (mW)	22.3	140	29.4	-	49.3/10.5[e]	165	**11.7**
FoM[&&]	-	10.97	11.82	27.33	25.71	3.49	**10.63**

[a] Simulation results.
[b] APD on chip.
[c] Programable.
[d] High gain mode.
[e] Two operation modes.

diode-connected MOS pair parallel-connected with the feedback resistor, which effectively suppresses output voltage pulse widening under high-input-current conditions. Simulation results demonstrate that the TIA with the proposed pulse widening suppression scheme achieves significant pulse widening suppression. Consequently, this PWS scheme simplifies the design of external gain control circuits and reduces system costs for processing large dynamic range echo signals in LiDAR receivers. In summary, the proposed TIA exhibits excellent overall performance and provides a versatile, cost-effective solution for pulsed ToF LiDAR systems.

CRediT author statement

Hao Zheng: Writing-Original draft preparation, Circuits design, Methodology. Yanming He: Reviewing and Editing. Xiayu Wang: Circuits simulation. Dong Li and Yanfei Liu: System modeling. Zhaoyuan Chen: Data curation. Rui Ma: Conceptualization, Supervision.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: Hao Zheng, Xiayu Wang, Dong Li, Yanfei Liu and Rui Ma reports financial support was provided by National Natural Science Foundation of China. Hao Zheng, Yanming He, Zhaoyuan Chen and Rui Ma reports financial support was provided by Natural Science Basic Research Program of Shaanxi Province. If there are other authors, they declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgments

This work was supported by the National Natural Science Foundation of China (62274182),in part by the National Natural Science Foundation of China under Grant 62134005, Grant 62571406, Grant 62574153, and the Natural Science Basic Research Program of Shaanxi under Grant 2025JC-YBQN-043, Grant 2024JC-JCQN-65.

Data availability

Data will be made available on request.

References

[1] Y. Li, J. Ibanez-Guzman, Lidar for autonomous driving: the principles, challenges, and trends for automotive lidar and perception systems, IEEE Signal Process. Mag. 37 (4) (2020) 50–61.
[2] H. Zheng, R. Ma, X. Wang, et al., A transimpedance amplifier with 99.8-dBΩ transimpedance gain and 400-MHz bandwidth for pulsed ToF lidar receiver applications, Microelectron. J. 165 (2025) 106845.
[3] D. Yoon, J.E. Joo, S.M. Park, Mirrored current-conveyor transimpedance amplifier for home monitoring LiDAR sensors, IEEE Sens. J. 21 (5) (2020) 5589–5597.
[4] S. Lee, B. Seo, S. Park, S.M. Park, An optoelectronic transmission-gate-based transimpedance amplifier in 180 nm CMOS, IEEE Sens. J. 25 (10) (2025) 16897–16904.
[5] S. Kurtti, A. Baharmast, J.P. Jansson, et al., A low-noise and wide dynamic range 15 MHz CMOS receiver for pulsed time-of-flight laser ranging, IEEE Sens. J. 21 (20) (2021) 22944–22955.
[6] H. Zheng, R. Ma, X. Wang, et al., A linear-array receiver AFE circuit embedded 8-to-1 multiplexer for direct ToF imaging LiDAR applications, IEEE Trans. Circuits Syst. I, Reg. Papers 69 (12) (2022) 5050–5058.
[7] K. Li, S. Su, Z. Huang, et al., A low walk error timing discrimination ASIC with rail-to-rail dynamic range and ICMR for pulsed ToF LiDAR receiver, IEEE Trans. Instrum. Meas. 74 (2025) 2005713.
[8] S. Kurtti, J. Kostamovaara, An integrated laser radar receiver channel utilizing a time-domain walk error compensation scheme, IEEE Trans. Instrum. Meas. 60 (1) (2011) 146–157.
[9] S. Kurtti, J. Nissinen, J. Kostamovaara, A wide dynamic range CMOS laser radar receiver with a time-domain walk error compensation scheme, IEEE Trans. Circuits Syst. I, Reg. Papers 64 (3) (2017) 550–561.
[10] M. Hintikka, J. Kostamovaara, A 700 MHz laser radar receiver realized in 0.18 μm HV-CMOS. Analog Integr, Circuits Signal Process 93 (2) (2017) 245–256.
[11] Y. Yang, H. Feng, Z. Yin, et al., An on-chip AC coupled AFE with asymmetric output stage for d-ToF LiDAR, IEEE Trans. Circuits Syst. II: Express Briefs 72 (1) (2025) 148–152.
[12] E. Säckinger, Broadband Circuits for Optical Fiber Communication, Wiley, New York, NY, USA, 2005.
[13] X. Wang, R. Ma, D. Li, et al., A wide dynamic range analog front-end with reconfigurable transimpedance amplifier for direct ToF LiDAR, IEEE Trans. Circuits Syst. II: Express Briefs 70 (3) (2023) 944–948.
[14] H. Zheng, R. Ma, M. Liu, et al., High sensitivity and wide dynamic range analog front-end circuits for pulsed TOF 4-D imaging LADAR receiver, IEEE Sens. J. 18 (8) (2018) 3114–3124.
[15] Y. Yang, X. Liu, R. Yang, et al., A low-power multimode eight-channel AFE for dToF LiDAR, in: 2024 IEEE International Symposium on Circuits and Systems (ISCAS), 2024.
[16] X. Tan, K. Li, J. Guo, A low-noise and high-accuracy transimpedance amplifier exploiting power-on-calibration technique for LiDAR, IEEE Trans. Instrum. Meas. 71 (2022) 2003810.
[17] H. Zheng, R. Ma, M. Liu, et al., A linear dynamic range receiver with timing discrimination for pulsed TOF imaging LADAR application, IEEE Trans. Instrum. Meas. 67 (11) (2018) 2684–2691.
[18] E. Sackinger, The transimpedance limit, IEEE Trans. Circuits Syst. I, Reg. Papers 57 (8) (2010) 1848–1856.
[19] Z. Zhang, Y. Zhang, Y. Xu, et al., A wideband low-noise linear LiDAR analog front-end achieving 1.6-GHz bandwidth, 2.7-pA/$Hz^{0.5}$ input-referred noise, and 103-dBΩ transimpedance gain, IEEE Solid-State Circuits Lett. 7 (2024) 131–134.
[20] C.J.M. Verhoeven, A. Staveren, G.L.E. Monna, et al., Structured Electronic Design: Negative Feedback Amplifiers, Kluwer, Norwell, MA, USA, 2003.
[21] Y. Chien, K. Fu, S. Liu, A 3–25 Gb/s four-channel receiver with noise-canceling TIA and power-scalable LA, IEEE Trans. Circuits Syst. II: Express Briefs 61 (11) (2014) 845–849.